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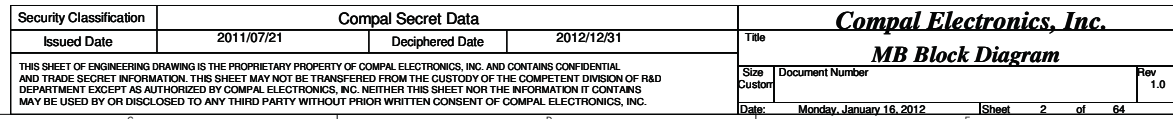
QIWY3 M/B Schematics Document

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13X

2011-12-23

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title		
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<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW	+1.5V	<div>+5VS</div> <div>+3VS</div> <div>+1.5VS</div> <div>+VCCSA</div> <div>+V1.5S_VCCP</div> <div>+CPU_CORE</div> <div>+VGA_CORE</div> <div>+GFX_CORE</div> <div>+1.8VS</div> <div>+1.05VS</div> <div>+0.75VS</div> <div>+3.3VS_VGA</div> <div>+1.5VS_VGA</div> <div>+1.05VS_VGA</div>
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

<div>SIGNAL</div> STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Vcc	3.3V +/- 5%					
Ra/Rc/Re	10K +/- 5%					
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Project	
0	0	0 V	0 V	0 V	QIWY3	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	QIWY3	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	QIWY3	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	QIWY3	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	QIWY4	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	QIWY4	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	QIWY4	PVT
7	NC	2.500 V	3.300 V	3.300 V	QIWY4	MP

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI	1	0
		2	1
		3	2
		4	3
EHCI2			4
			5
			6
			7
			8
			9
			10
EHCI2			11
			12
			13

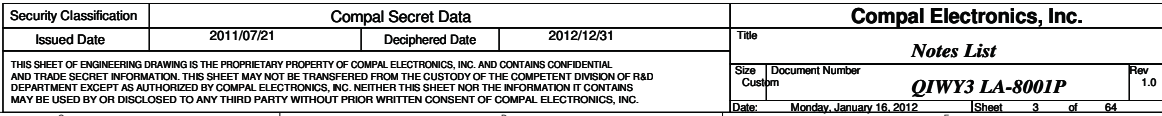
BOM Structure	BTO Item
OPTI@	OPTIMUS part
HDMI@	HDMI part
TV@	TV module part
CHG@	USB charger part
NOCHG@	No USB charger part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
S1G@	X76 P/N for Samsun VRAM 1G
S2G@	X76 P/N for Samsun VRAM 2G
H1G@	X76 P/N for Hynix VRAM 1G
H2G@	X76 P/N for Hynix VRAM 2G
GL@	N13P-GL part
GT@	N13P-GT part
GE@	N13E-GE part
GTGE@	N13P-GT&N13E-GE common part
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
1403@	EMC1403 thermal part
2103@	EMC2103 thermal part
KBL@	K/B Light part
ME@	ME part
@	Unpop

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

Device	Device	Address
Smart Battery	Thermal Sensor EMC1403-2	1001_101xb

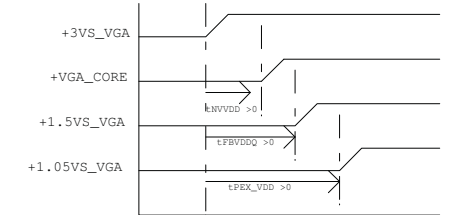
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



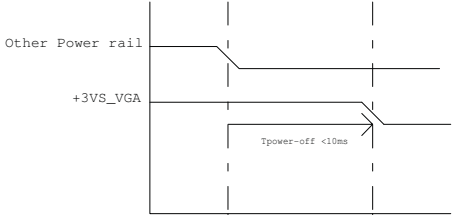
Hot plug detect for IFP link C

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description	
GPIO0	OUT	-	GPU VID4	
GPIO1	OUT	-	GPU VID3	
GPIO2	OUT	N/A		
GPIO3	OUT	N/A		
GPIO4	OUT	N/A		
GPIO5	OUT	-	GPU VID1	
GPIO6	OUT	-	GPU VID2	
GPIO7	OUT	N/A		
GPIO8	I/O	-	Thermal Catastrophic Over Temperature	
GPIO9	OUT	-	GC6 event	
GPIO10	OUT	-	Memory VREF Control	
GPIO11	OUT	-	GPU VID0	
GPIO12	IN		AC Power Detect Input	(10K pull High)
GPIO13	OUT	-	GPU VID5	
GPIO14	OUT	N/A		
GPIO15	IN	N/A	(100K pull low)	
GPIO16	OUT	N/A		
GPIO17	IN	N/A		
GPIO18	IN	N/A		
GPIO19	IN	N/A		



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

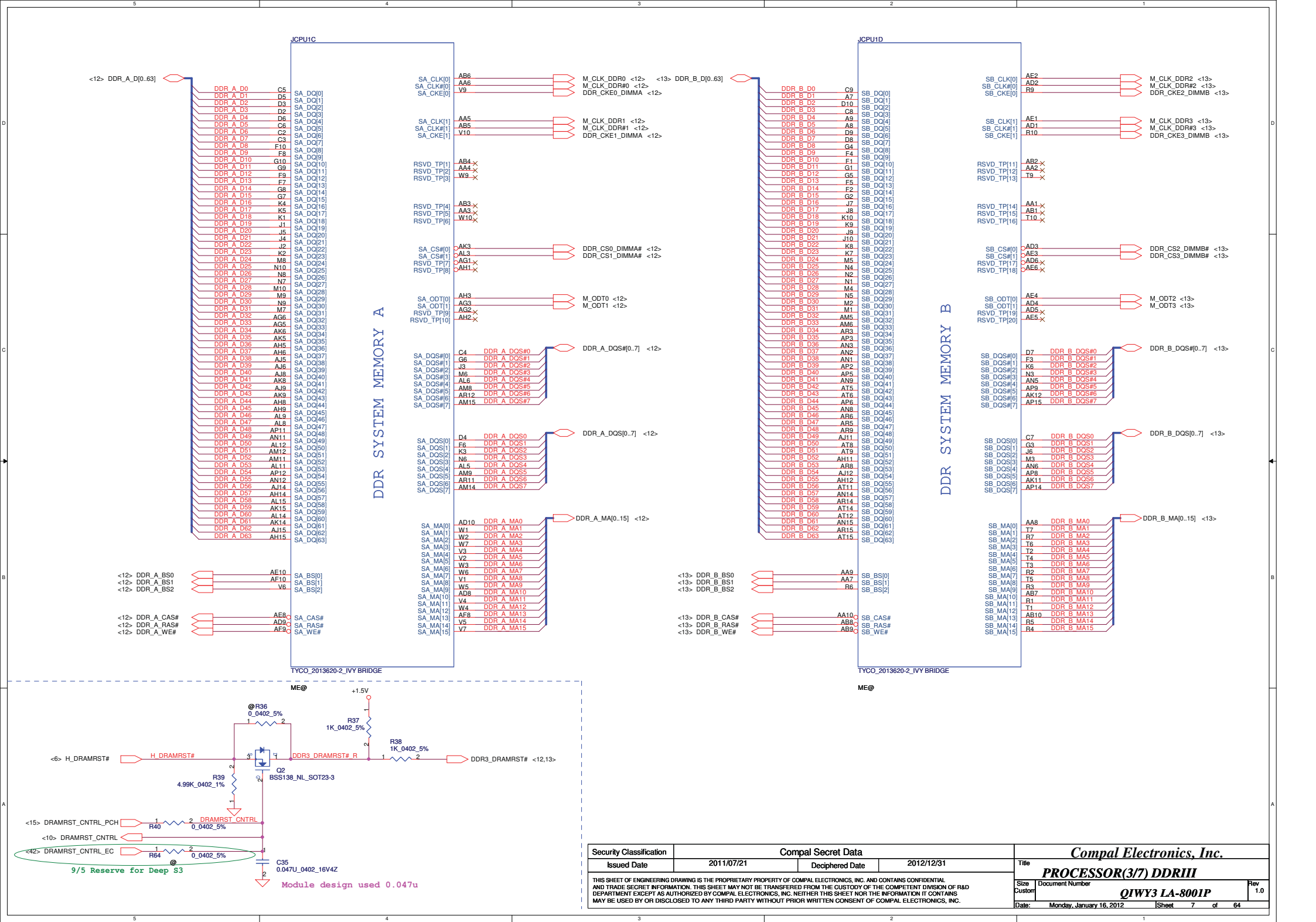
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_FLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB
N13E-GE (28nm)	0x0FDB
N13P-GL1 (40nm)	0x0DE9

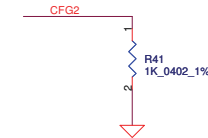
GPU	ROM_SO	ROM_SCLK	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
N13P-GT	PU 10K	PU 5K	PD 45K	PD 5K	PD 10K	PD 35K	PU 45K
N13E-GE	PU 10K	PU 5K	PD 45K	PD 5K	PD 25K	PD 35K	PU 45K
N13P-GL	PD 10K	PD 15K	NC	NC	PU 10K	PD 45K	PU 45K

GPU		N13P-GT	N13E-GE	N13P-GL
FB Memory (GDDR5)		ROM_SI	ROM_SI	ROM_SI
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K	PD 45K	PD 45K
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K	PD 35K	PD 35K
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K	PD 30K	PD 30K
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K	PD 25K	PD 25K

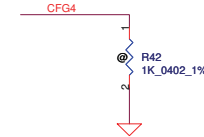
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Issued Date		2011/07/21	Deciphered Date	2012/12/31	Title	
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					Size	Document Number
						QIWAY3 LA-8001P
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					Rev	1.0



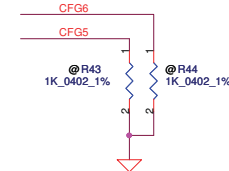
CFG Straps for Processor



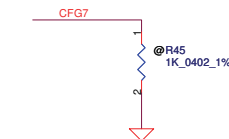
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



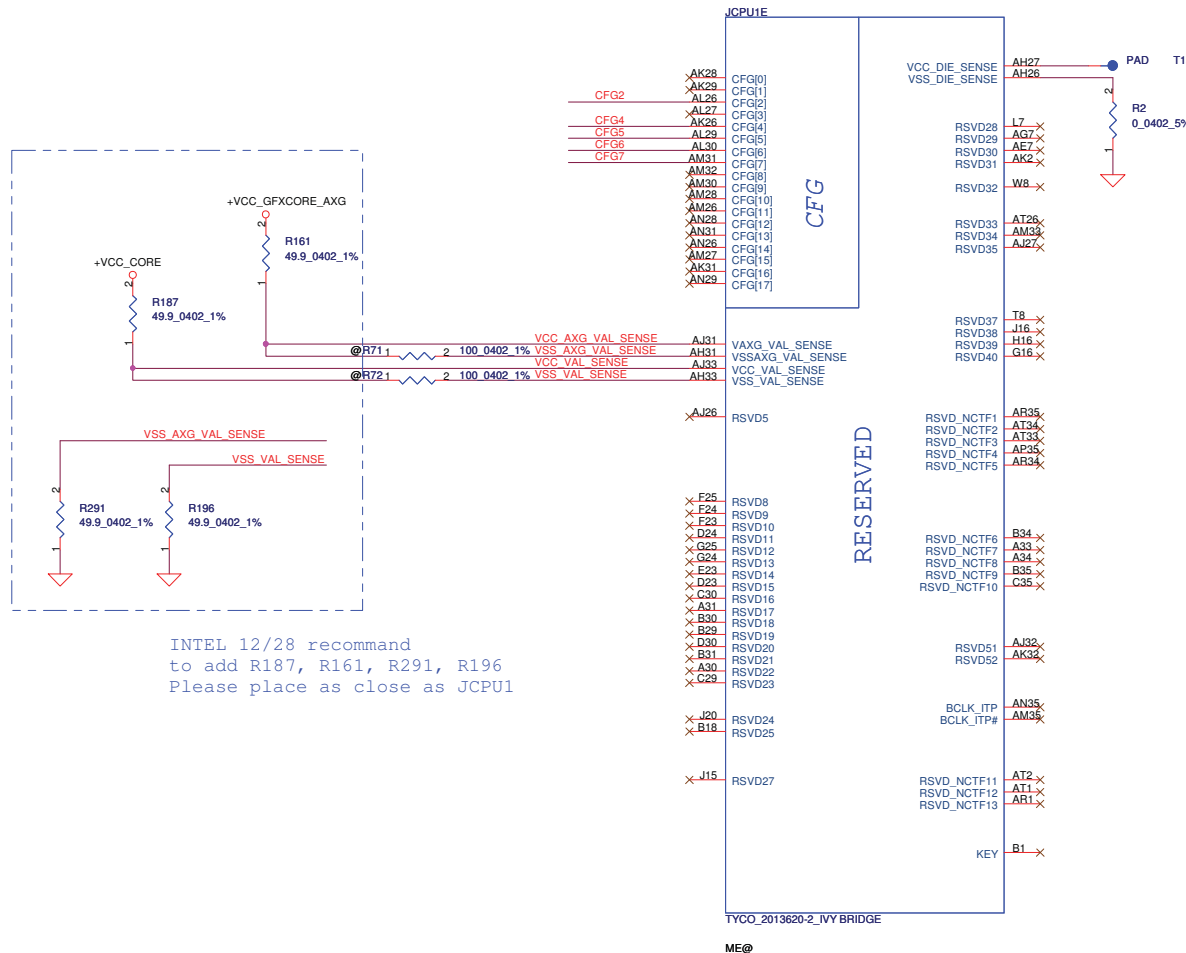
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

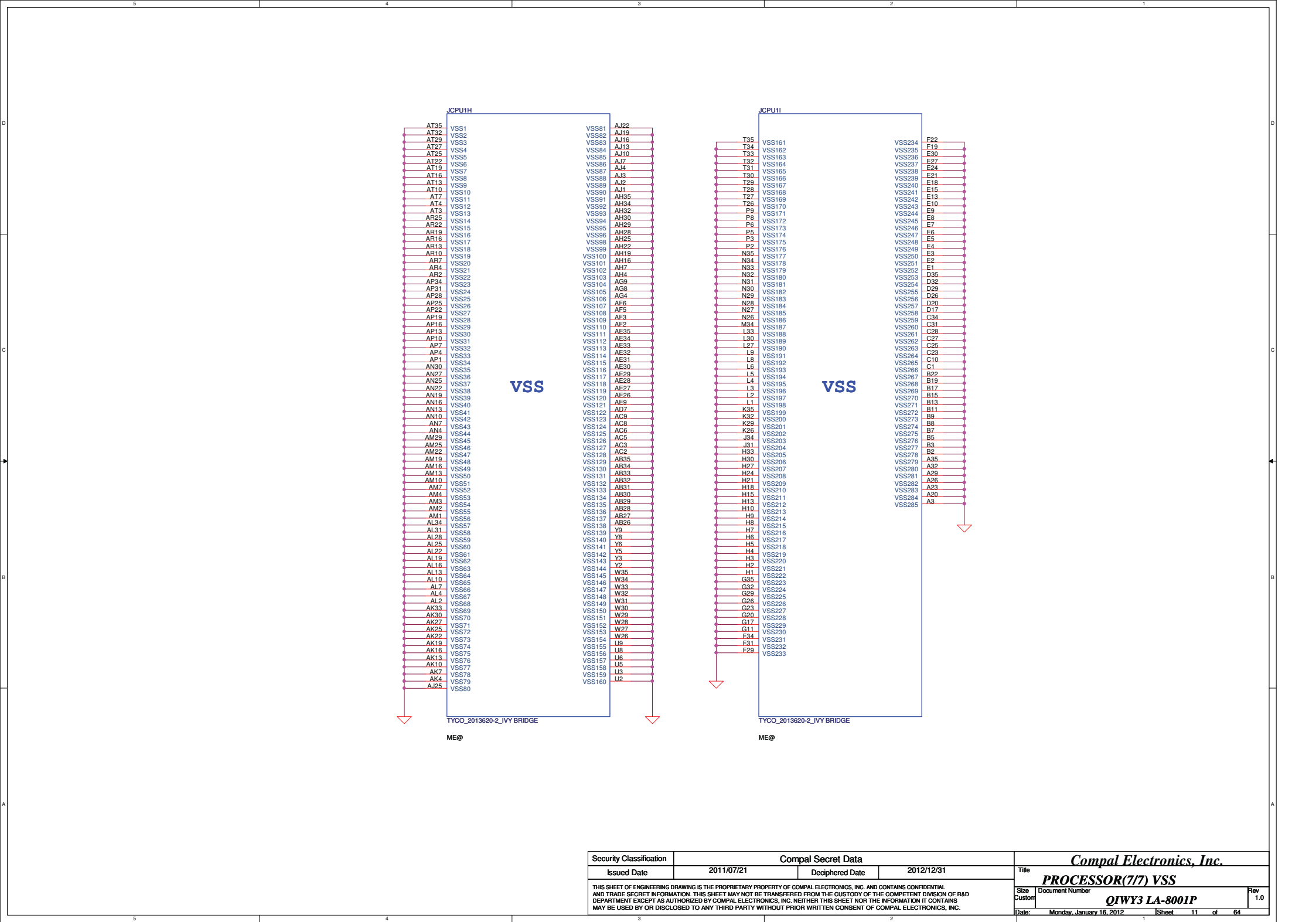


PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

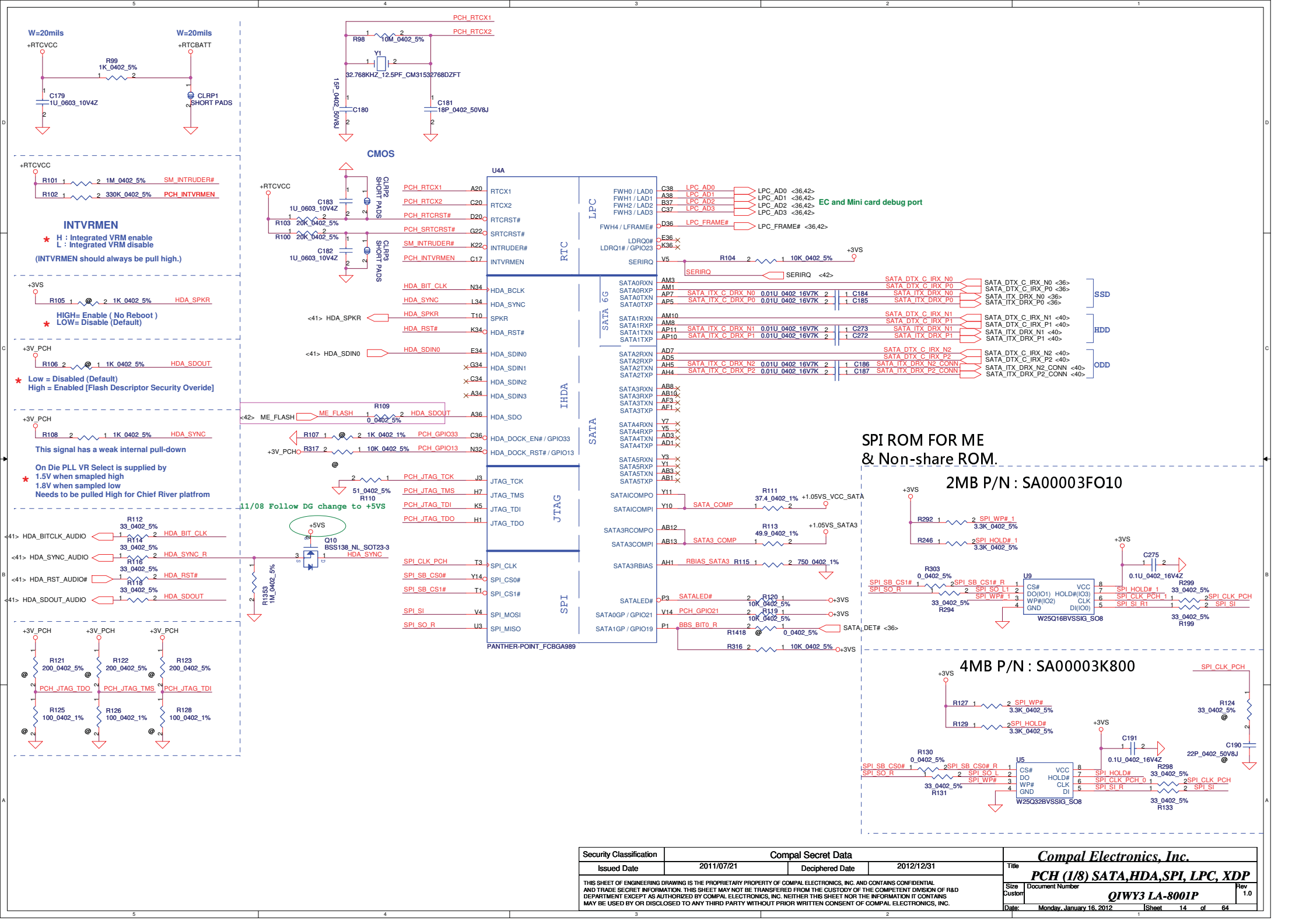


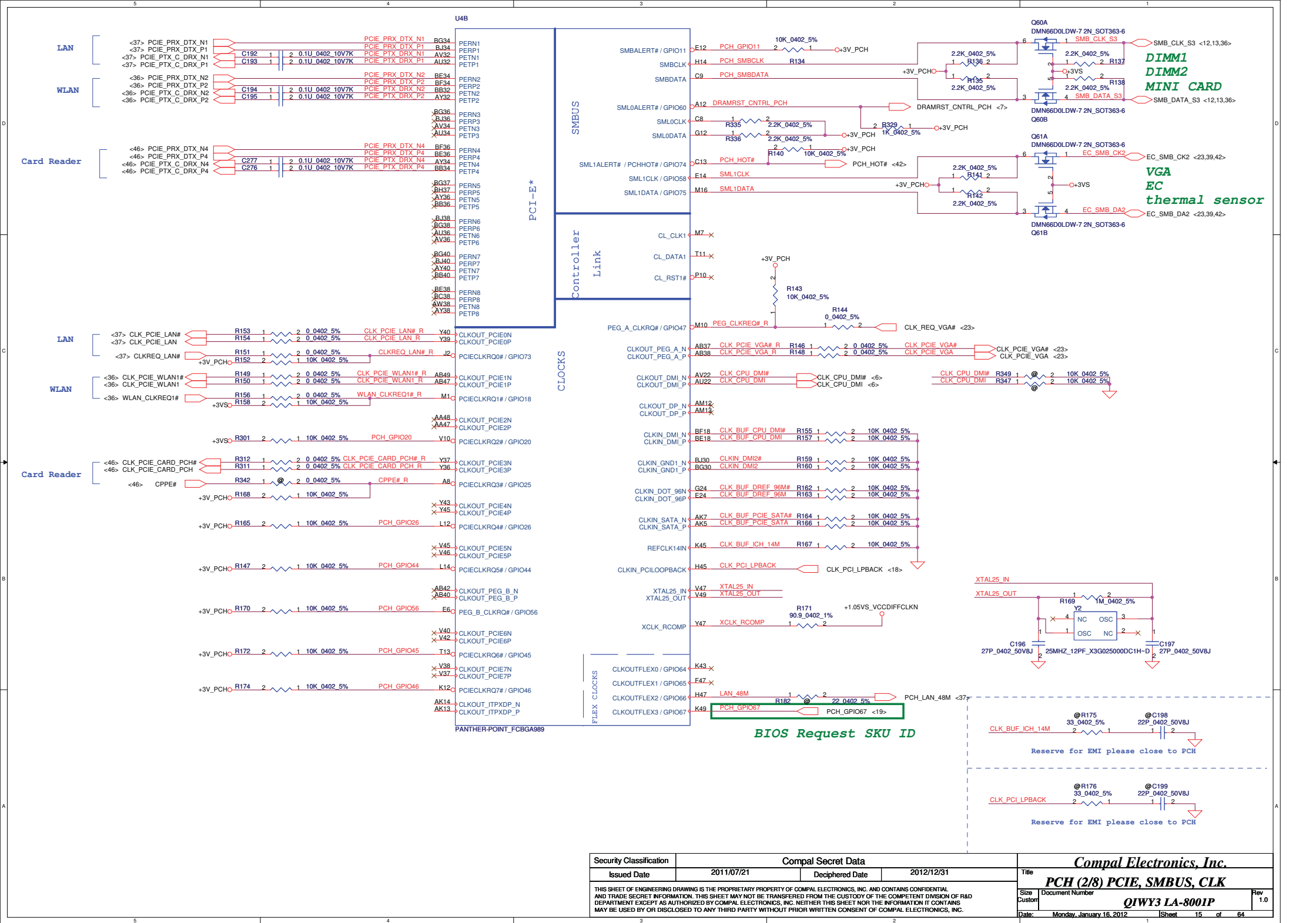
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

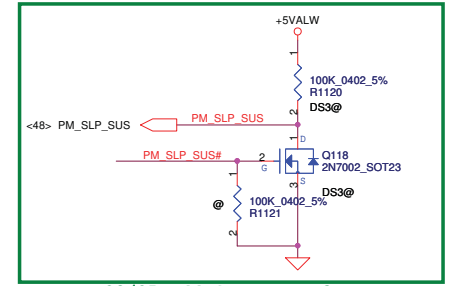
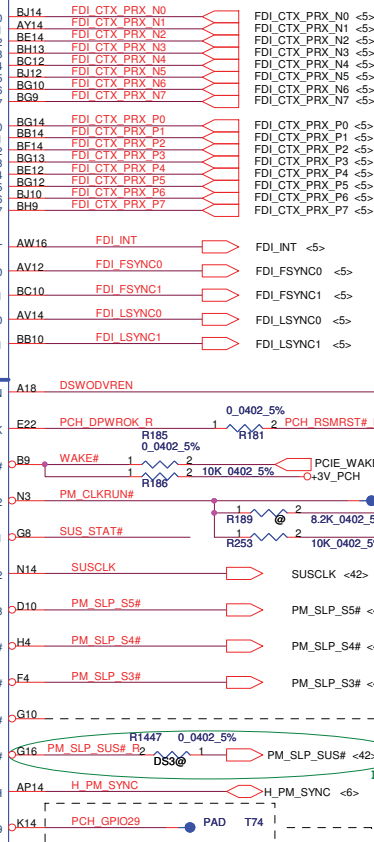
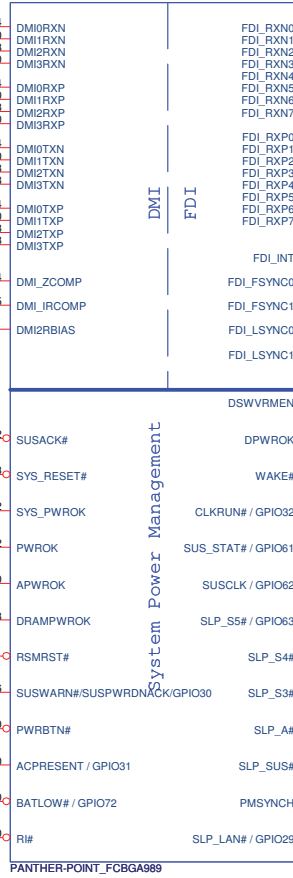
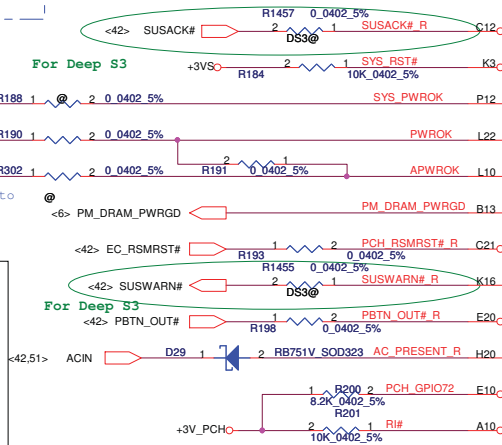
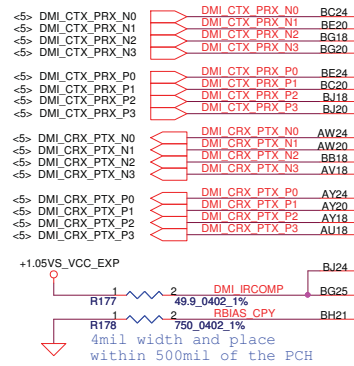
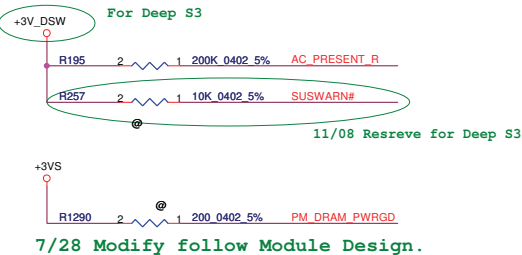
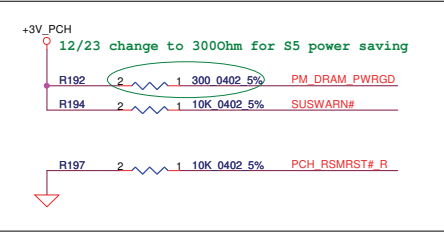
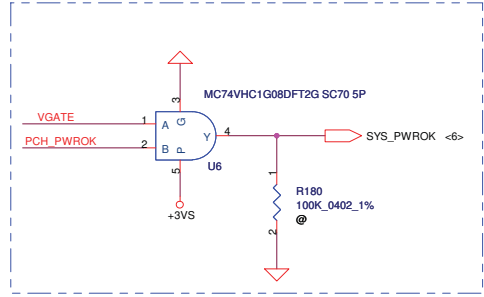




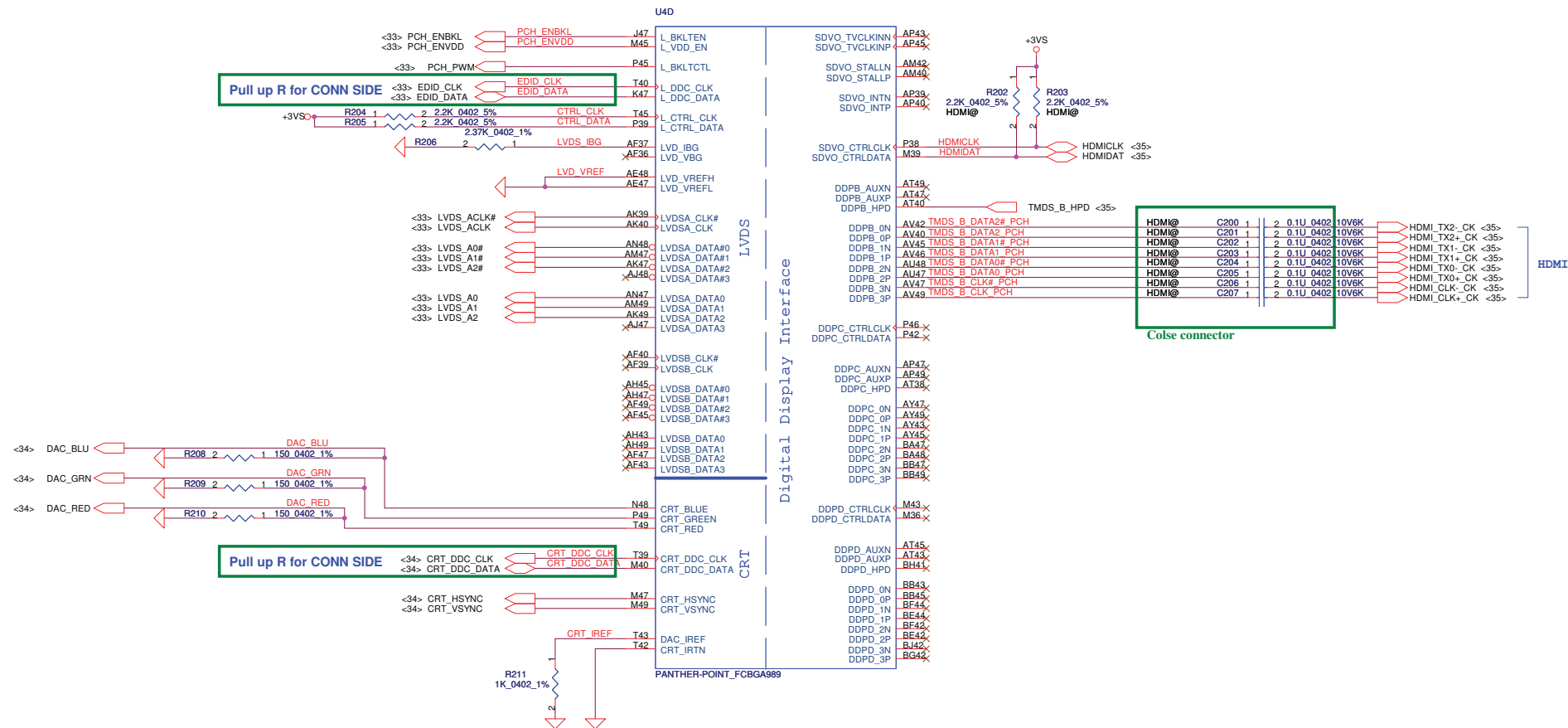






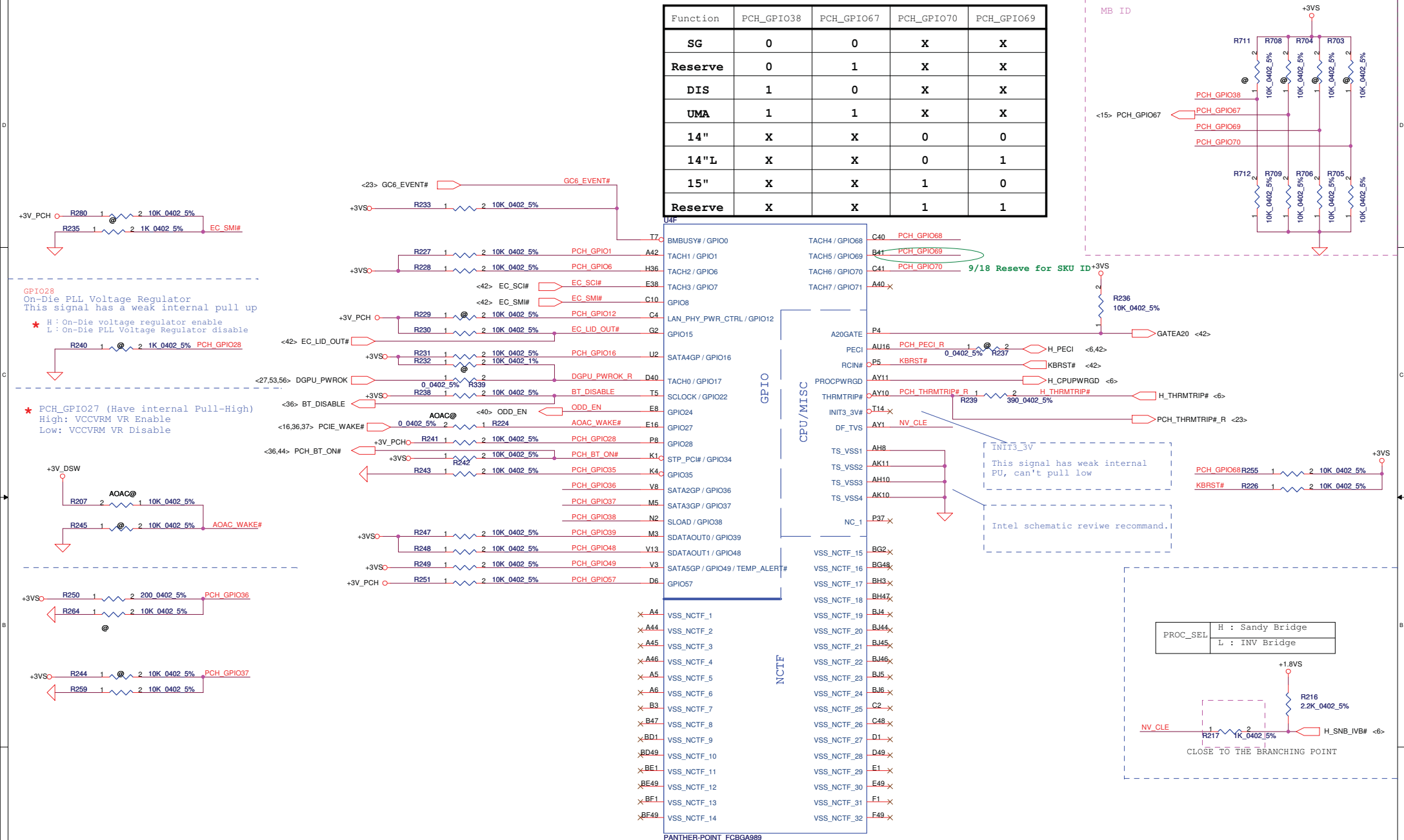
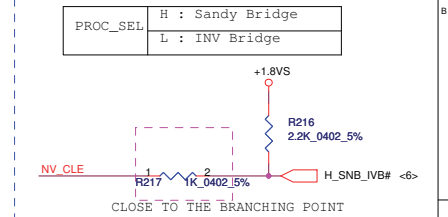
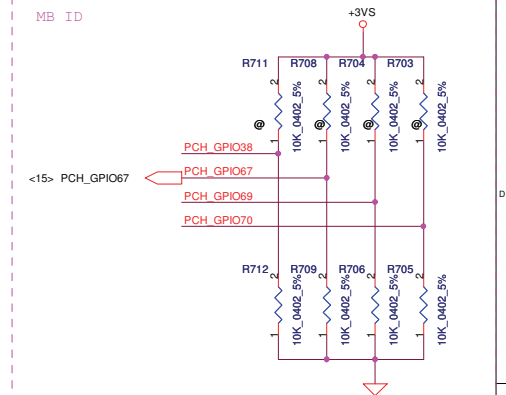


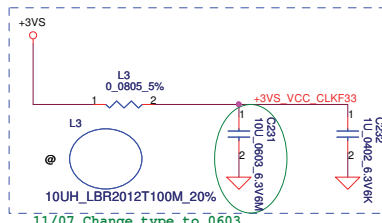
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Deciphered Date				2012/12/31				QIWIY3 LA-8001P			
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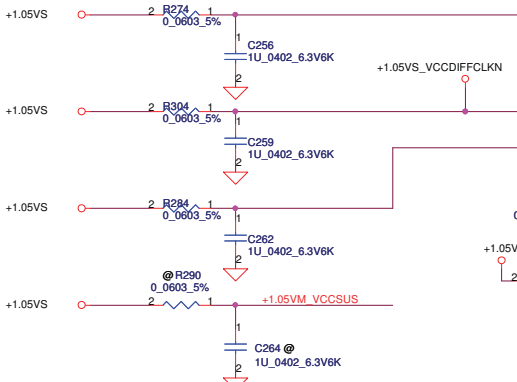
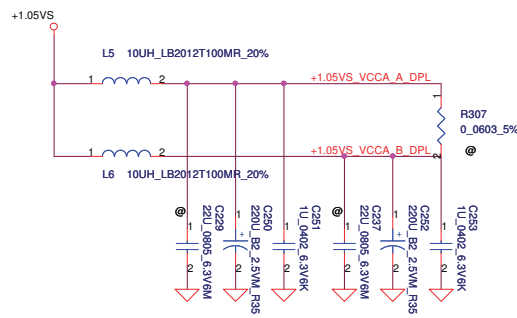
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Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70	PCH_GPIO69
SG	0	0	X	X
Reserve	0	1	X	X
DIS	1	0	X	X
UMA	1	1	X	X
14"	X	X	0	0
14"L	X	X	0	1
15"	X	X	1	0
Reserve	X	X	1	1

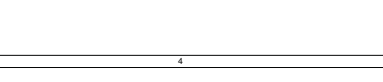
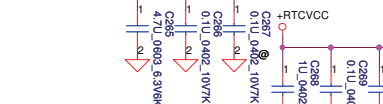
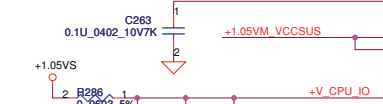
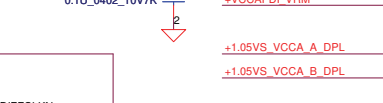
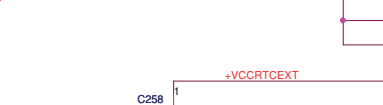
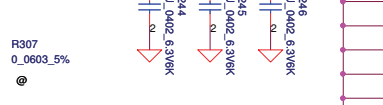
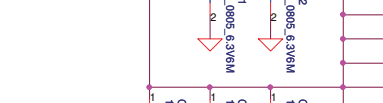
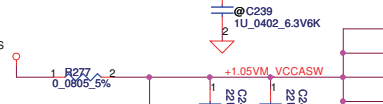
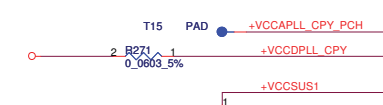
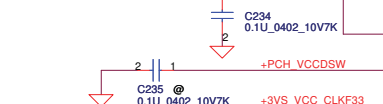
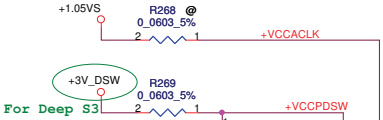




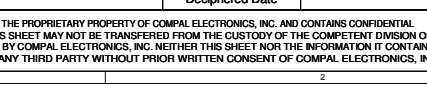
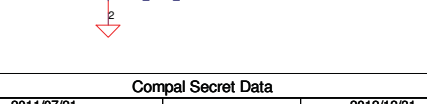
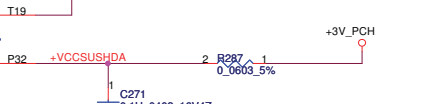
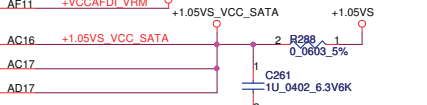
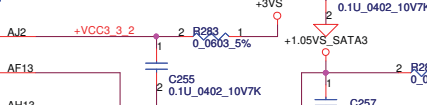
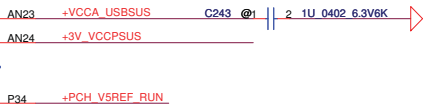
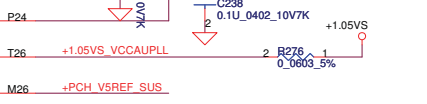
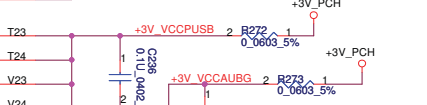
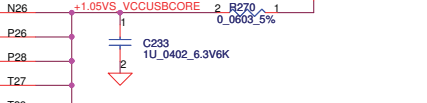
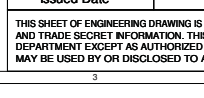
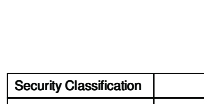
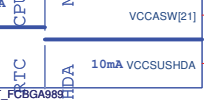
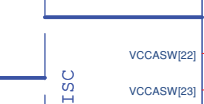
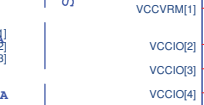
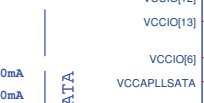
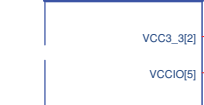
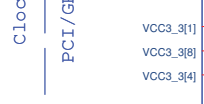
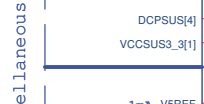
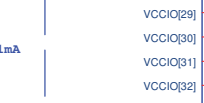
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA



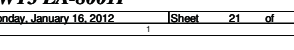
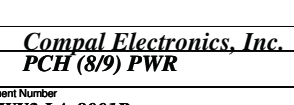
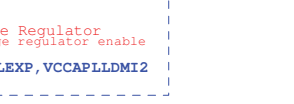
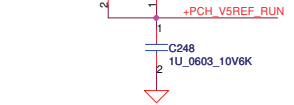
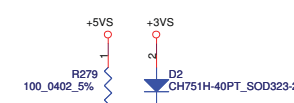
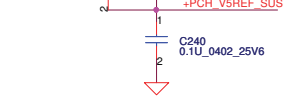
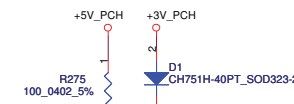
Have internal VRM



POWER

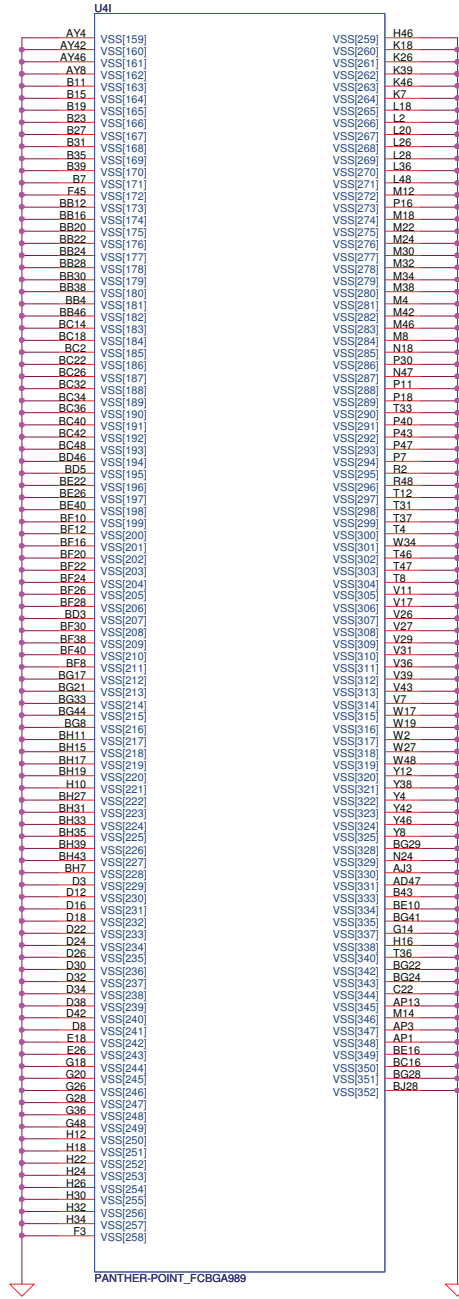
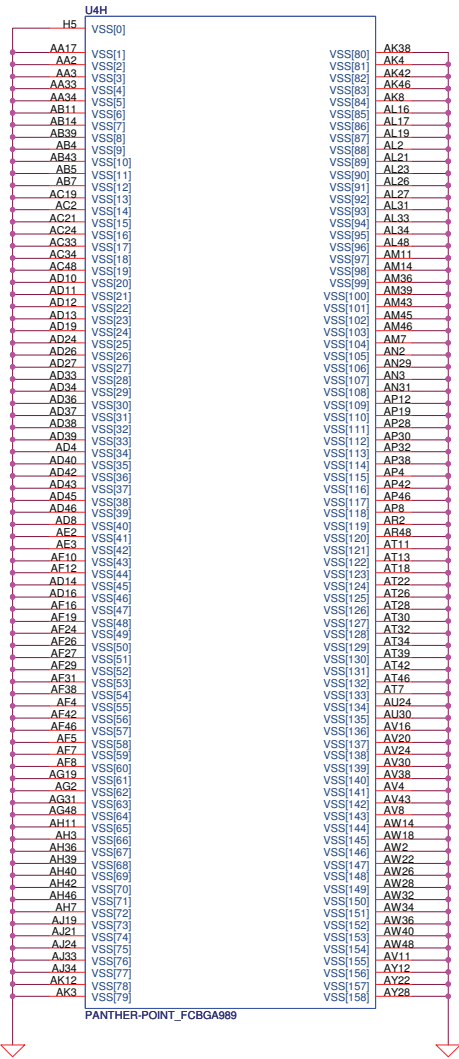


VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

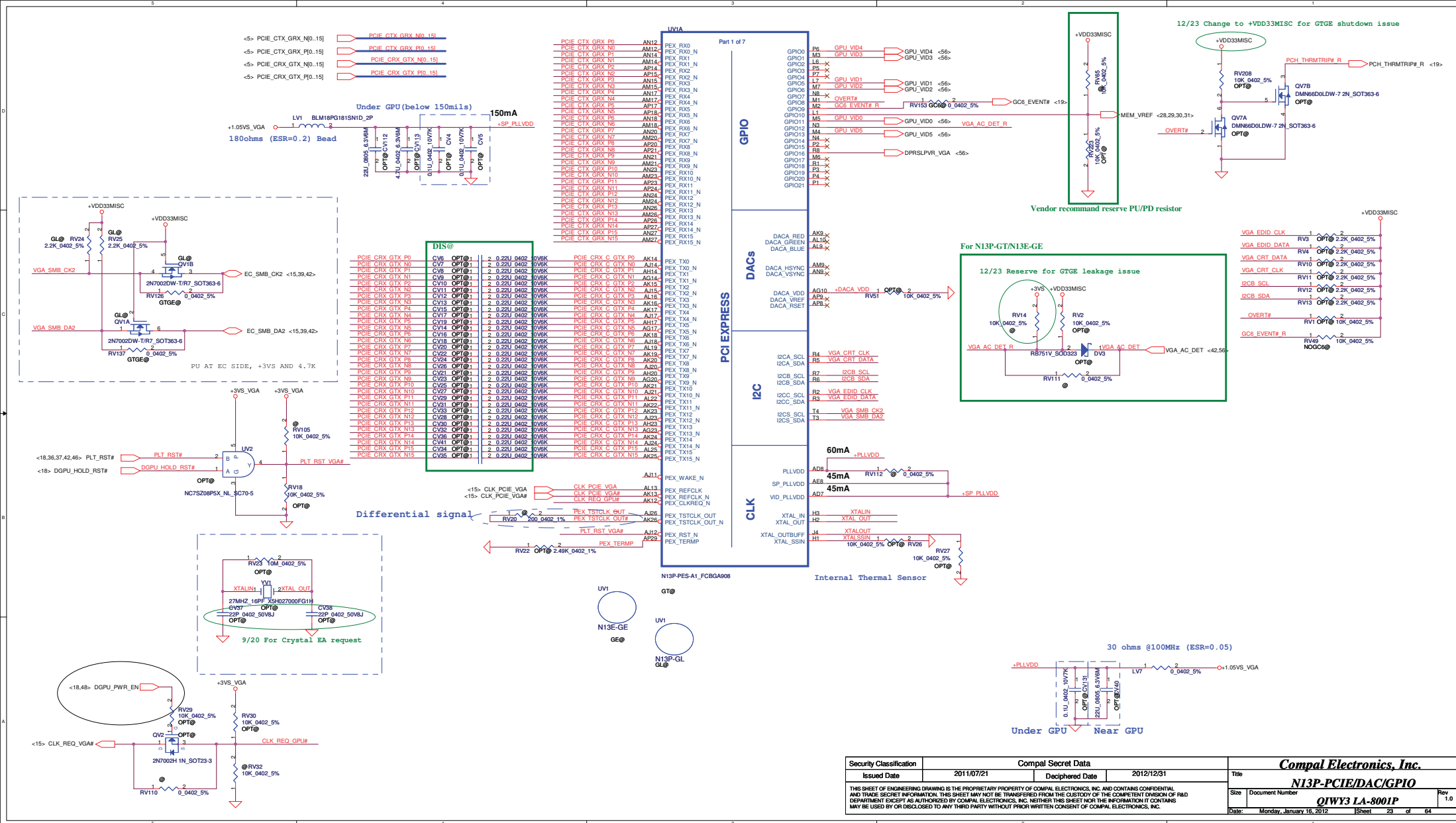


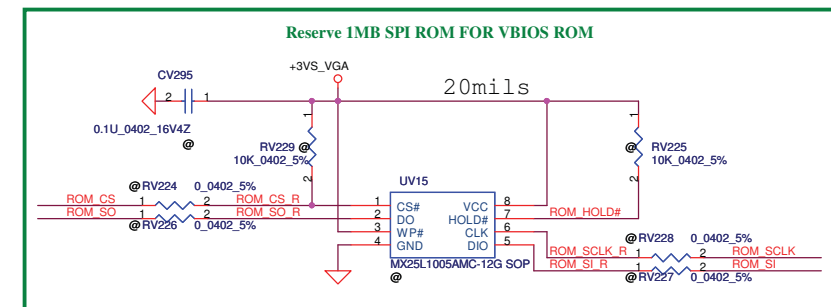
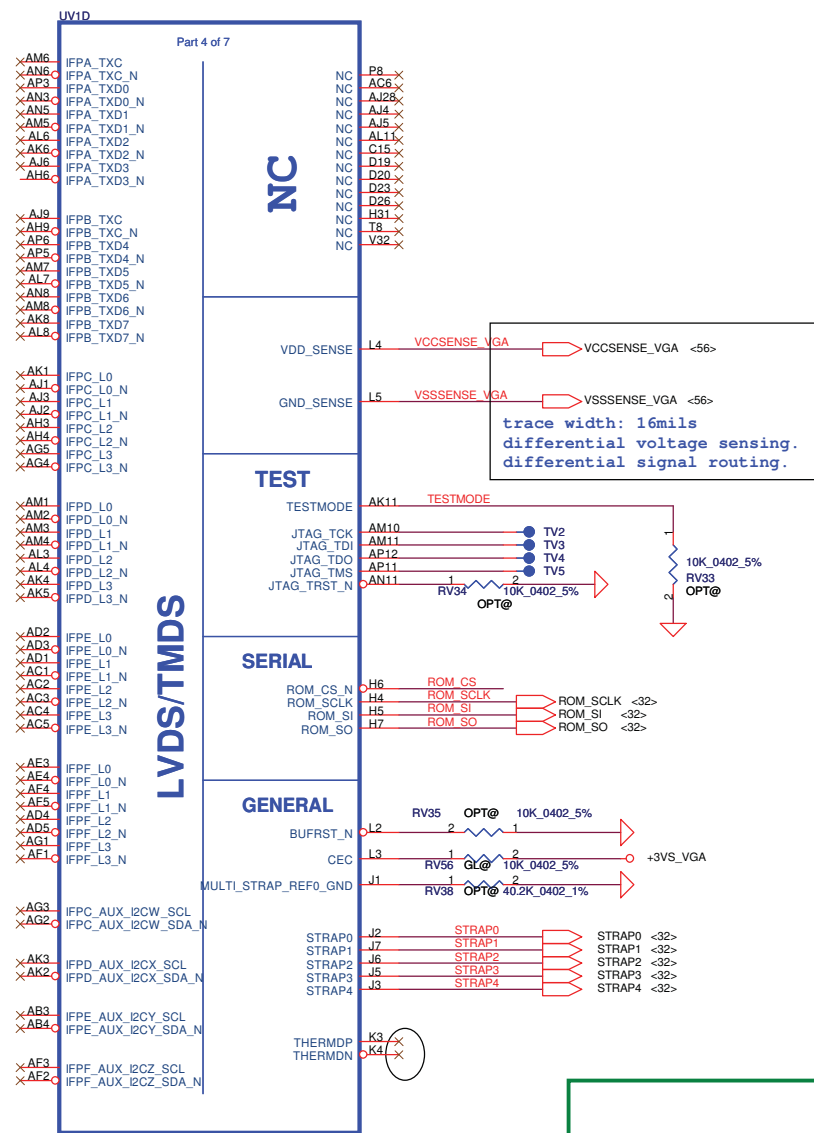
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Issued Date				2011/07/21				PCH (8/9) PWR			
Deciphered Date				2012/12/31				QIWIY3 LA-8001P			
Title				Size				Rev			
Document Number				Monday, January 16, 2012				Sheet 21 of 64			
Date				1				1.0			

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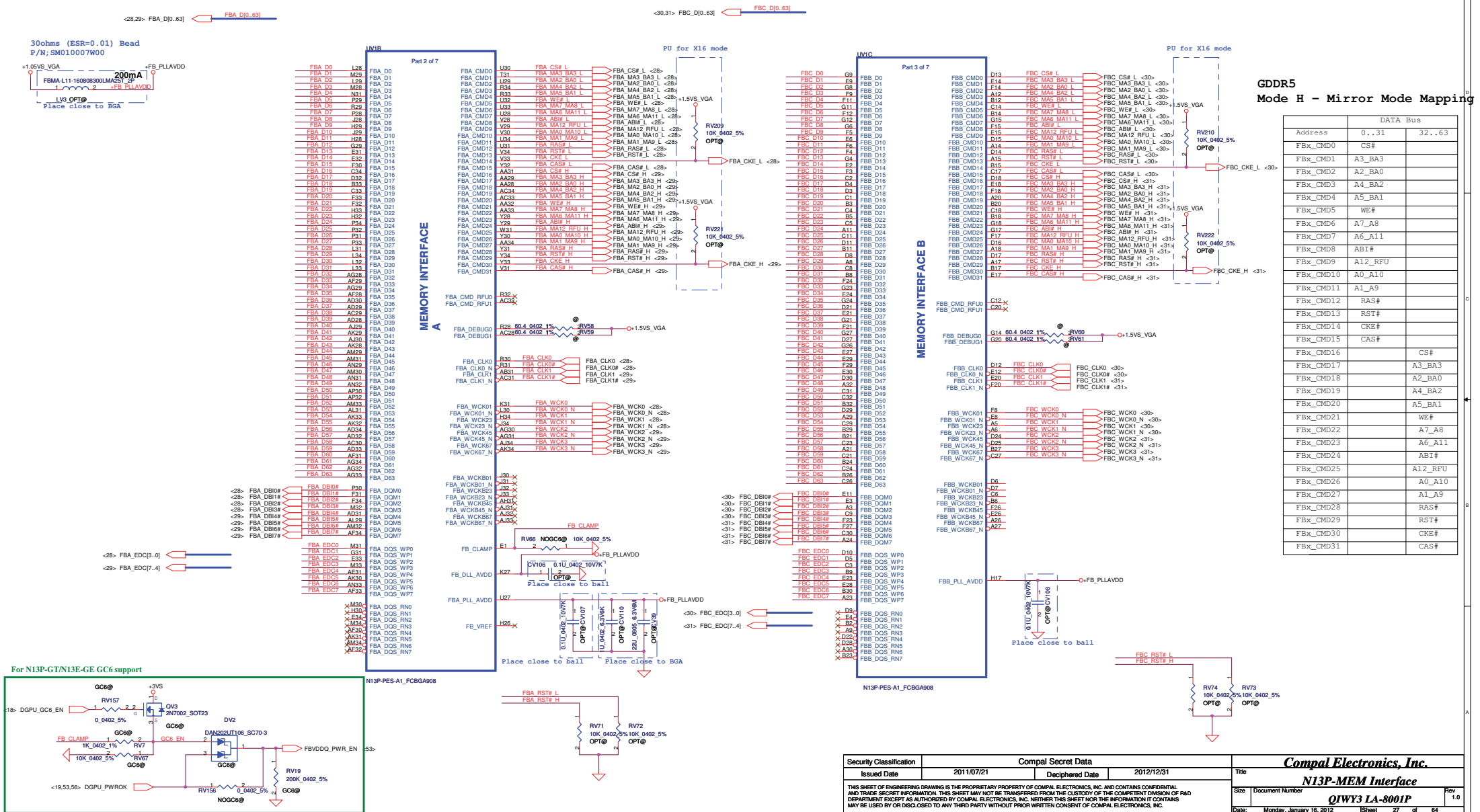


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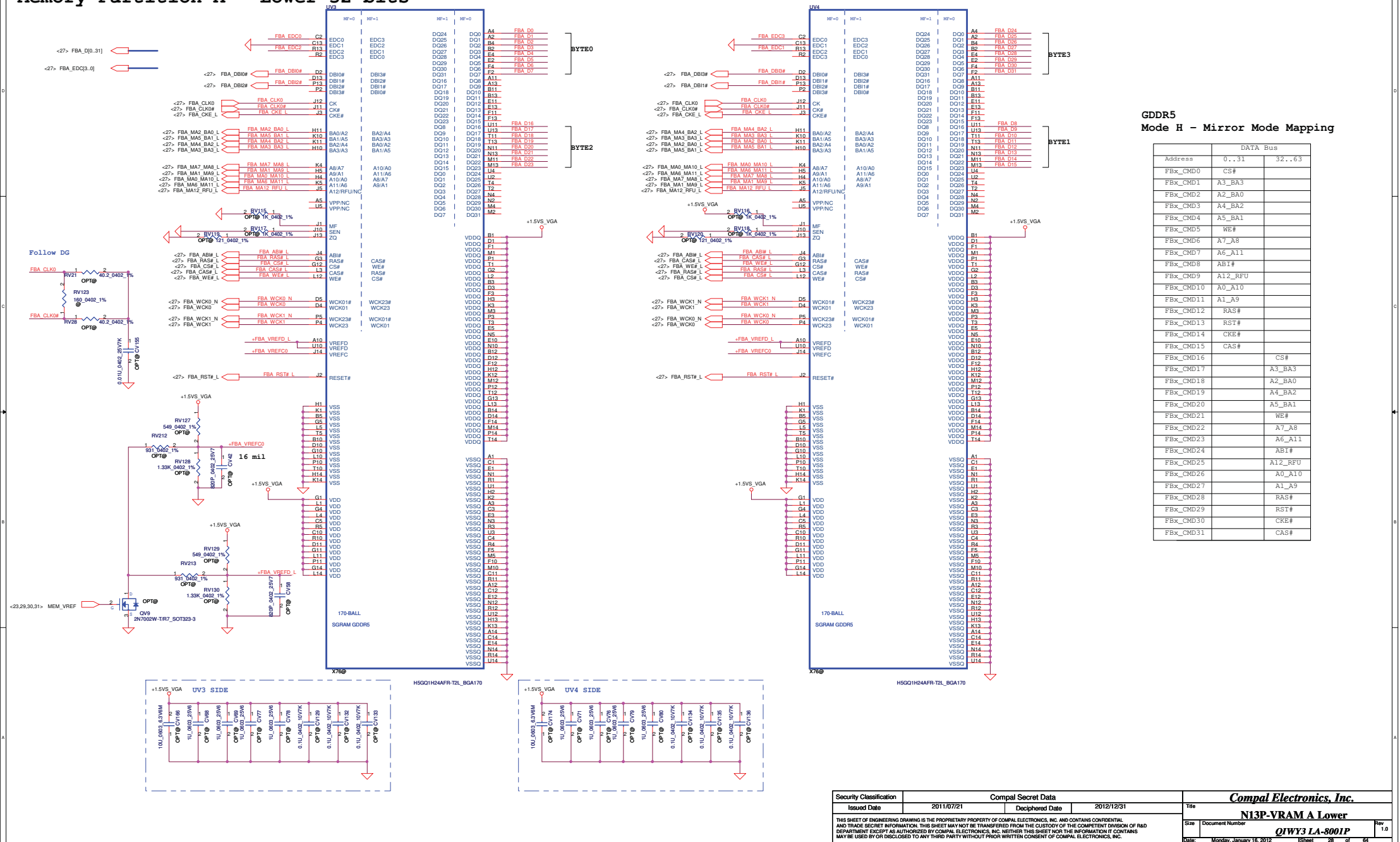
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Size	Document Number	QIWIY3 LA-8001P		Date	Monday, January 16, 2012	Rev 1.0
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GDDR5
Mode H - Mirror Mode Mapping

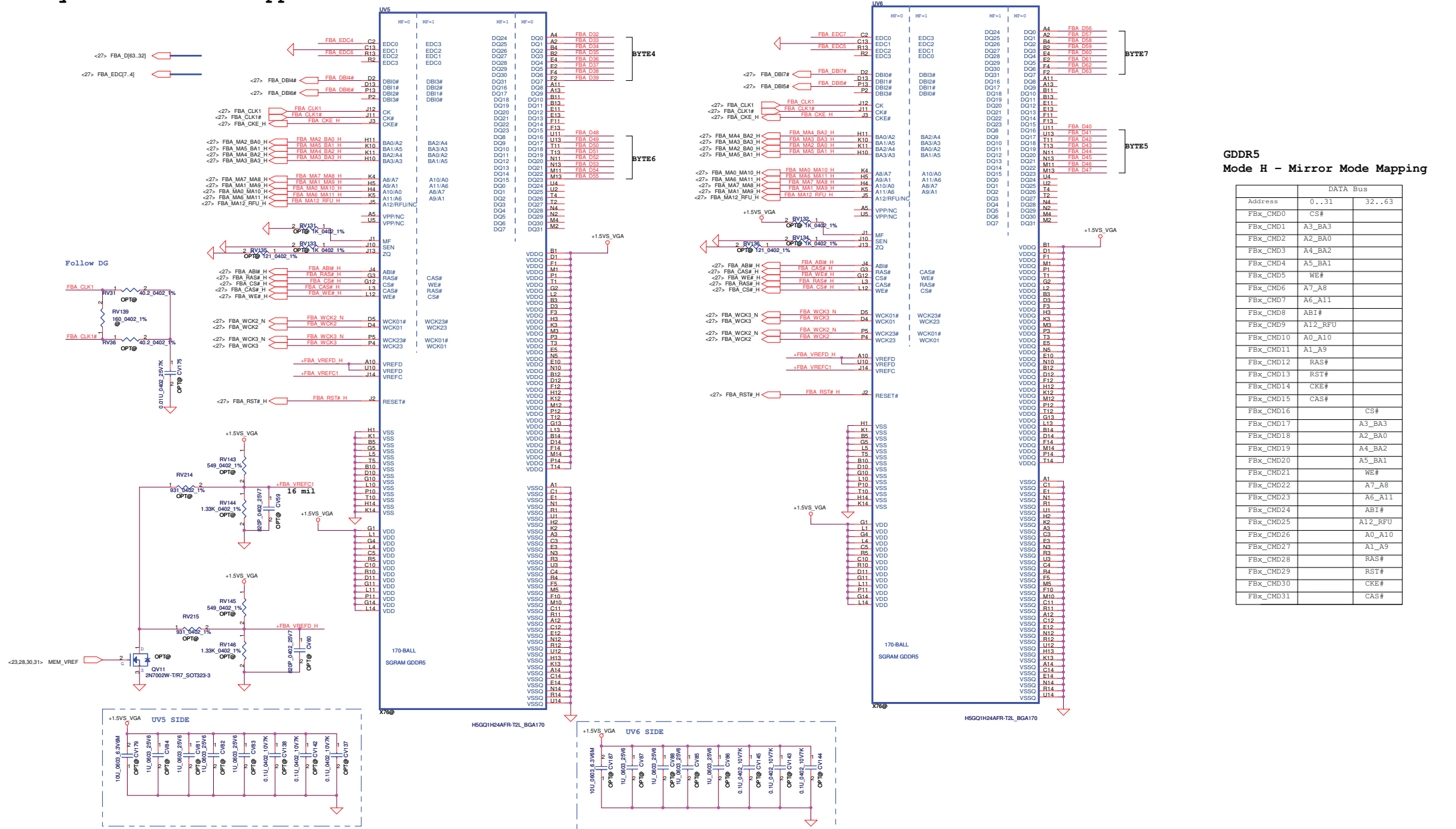
Address	DATA Bus
FBx_CMD0	0..31
FBx_CMD1	CS#
FBx_CMD2	A3_BA3
FBx_CMD3	A2_BA0
FBx_CMD4	A4_BA2
FBx_CMD5	A5_BA1
FBx_CMD6	WE#
FBx_CMD7	A6_A11
FBx_CMD8	AB1#
FBx_CMD9	A12_RFU
FBx_CMD10	A0_A10
FBx_CMD11	A1_A9
FBx_CMD12	RAS#
FBx_CMD13	RST#
FBx_CMD14	CKE#
FBx_CMD15	CAS#
FBx_CMD16	CS#
FBx_CMD17	A3_BA3
FBx_CMD18	A2_BA0
FBx_CMD19	A4_BA2
FBx_CMD20	A5_BA1
FBx_CMD21	WE#
FBx_CMD22	A7_A8
FBx_CMD23	A6_A11
FBx_CMD24	AB1#
FBx_CMD25	A12_RFU
FBx_CMD26	A0_A10
FBx_CMD27	A1_A9
FBx_CMD28	RAS#
FBx_CMD29	RST#
FBx_CMD30	CKE#
FBx_CMD31	CAS#

Memory Partition A - Lower 32 bits



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Memory Partition A - Upper 32 bits



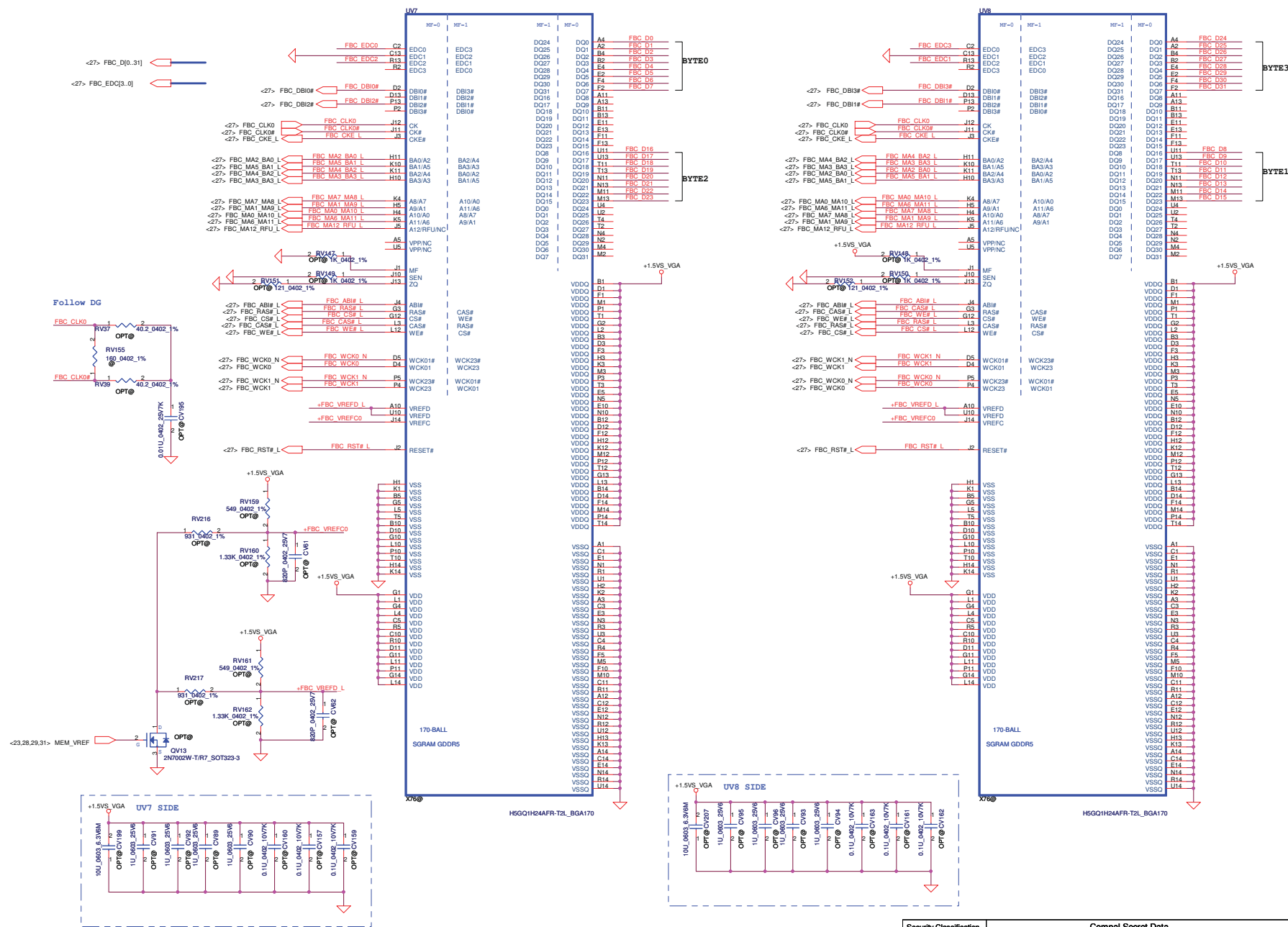
ADDR5

Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	AB1#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RAS#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17		A3_BA3
FbX_CMD18		A2_BA0
FbX_CMD19		A4_BA2
FbX_CMD20		A5_BA1
FbX_CMD21		WE#
FbX_CMD22		A7_A8
FbX_CMD23		A6_A11
FbX_CMD24		AB1#
FbX_CMD25		A12_RFU
FbX_CMD26		A0_A10
FbX_CMD27		A1_A9
FbX_CMD28		RAS#
FbX_CMD29		RST#
FbX_CMD30		CKE#
FbX_CMD31		CAS#

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Memory Partition C - Lower 32 bits

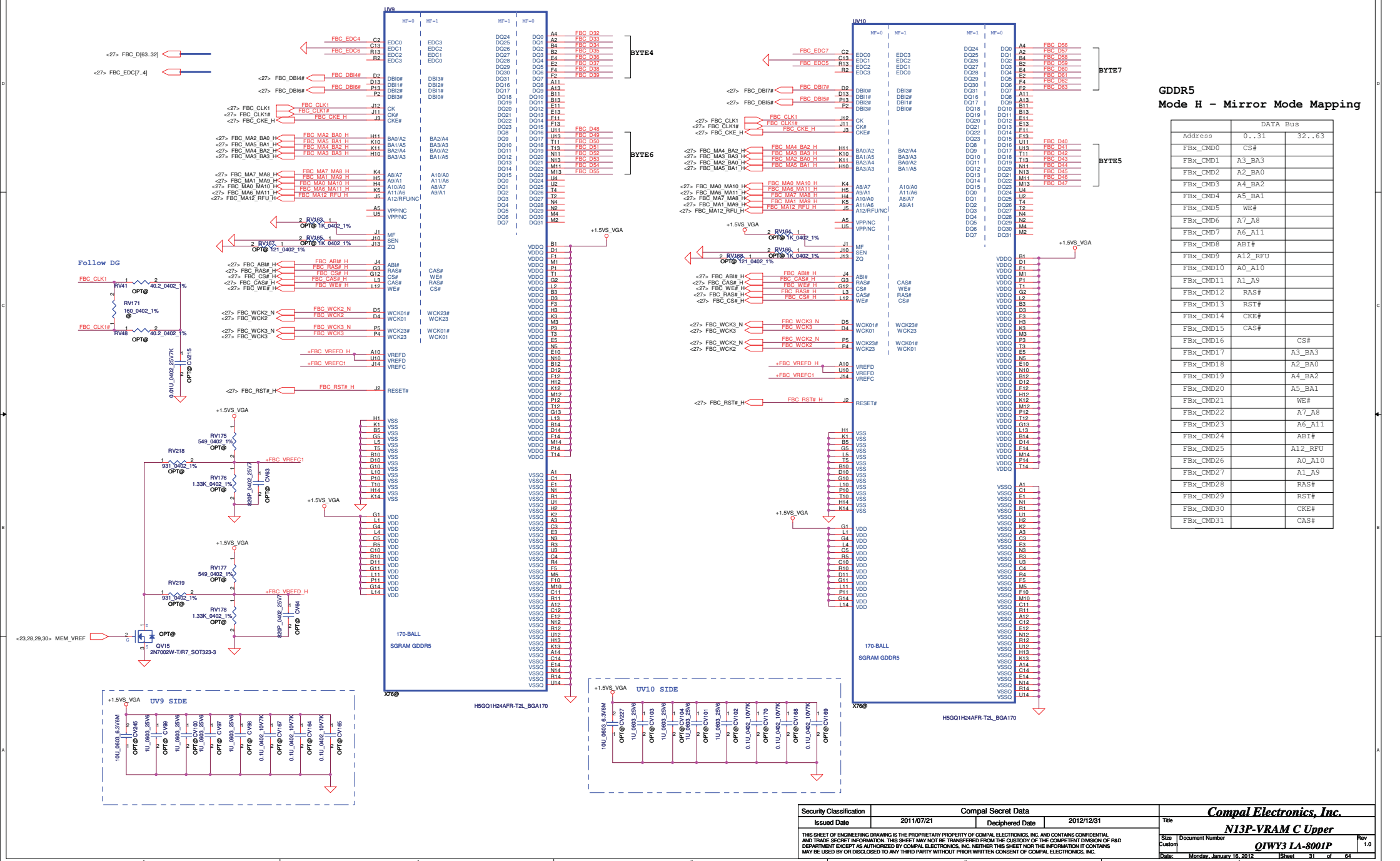


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		AB1#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

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Date: Monday, January 16, 2012			Sheet 39	Rev 1.0

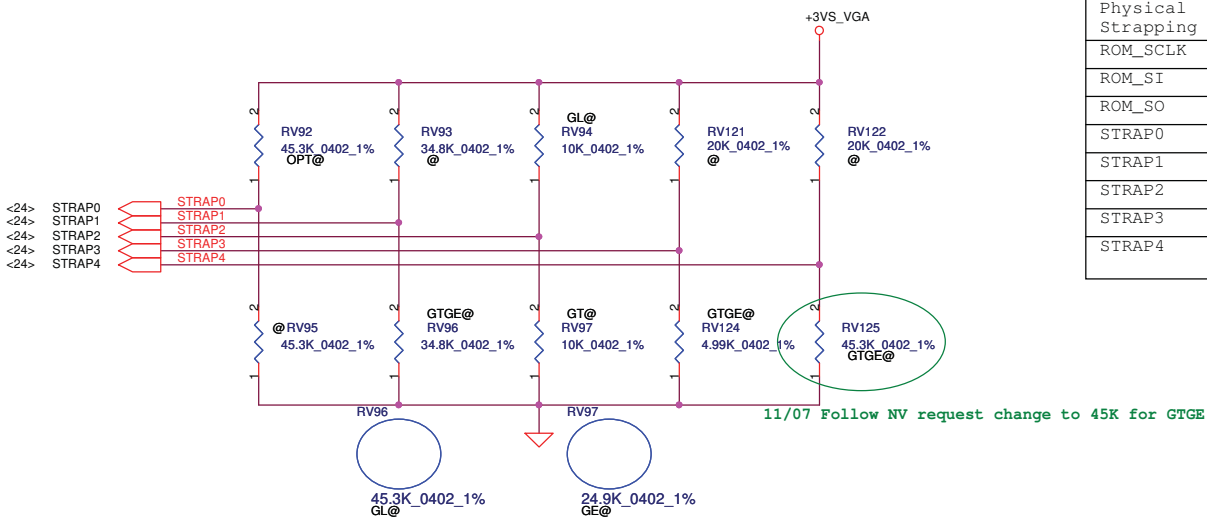
Memory Partition C - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

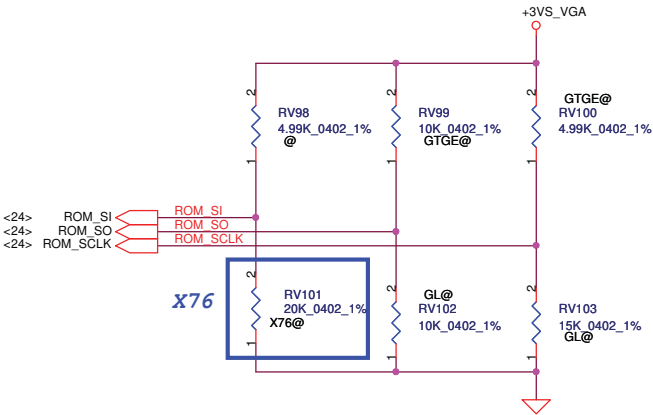
	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	ABI#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		ABI#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



3GIO_PADCFG		XCLK_417	
3GIO_PADCFG[3:0]		0	277MHz (Default)
0110	Notebook Default	1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

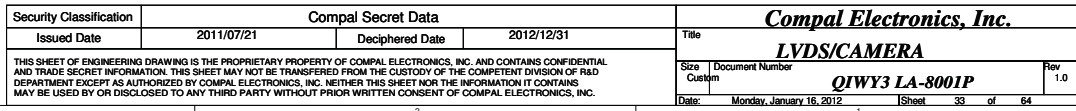
USER Straps	
User[3:0]	
1000-1100	Customer defined

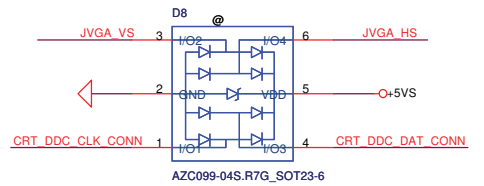
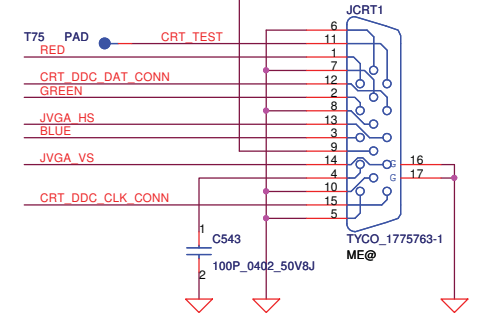
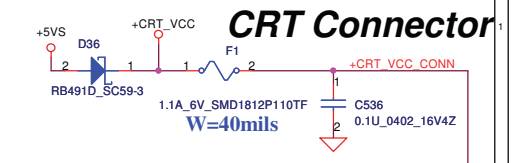
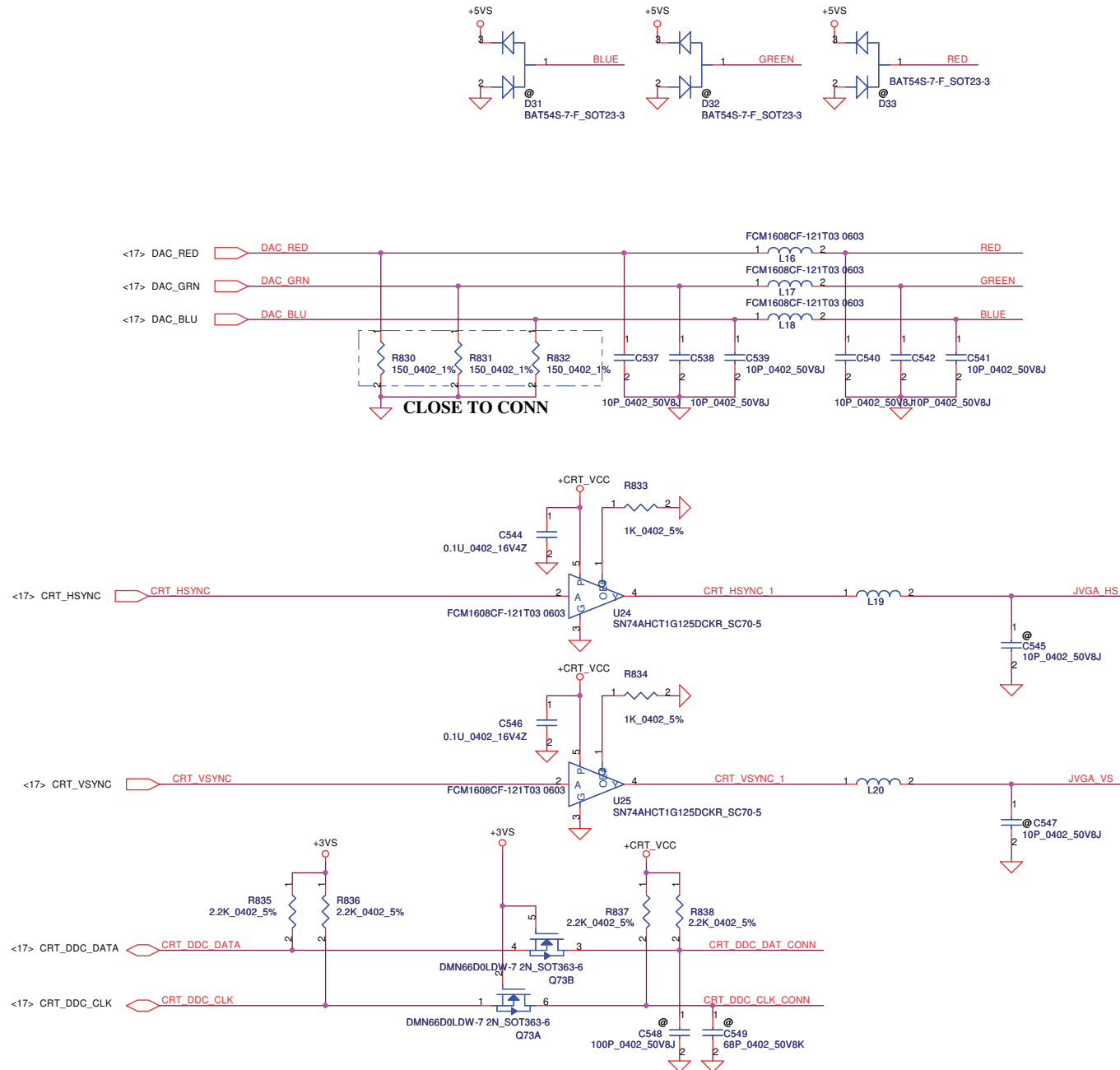
FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

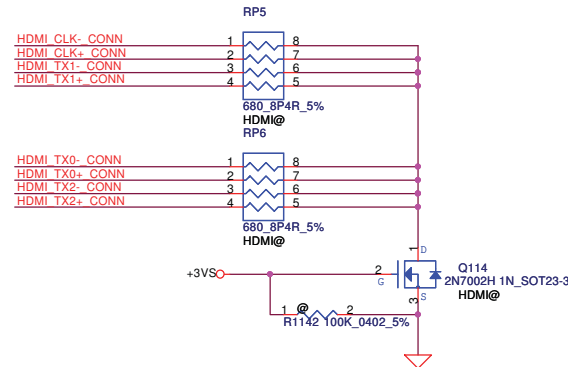
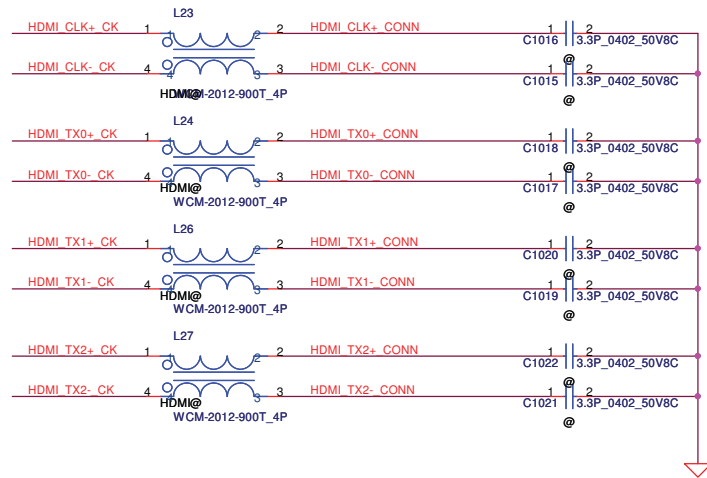
PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

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				Date:	Monday, January 16, 2012	Sheet 32 of 64

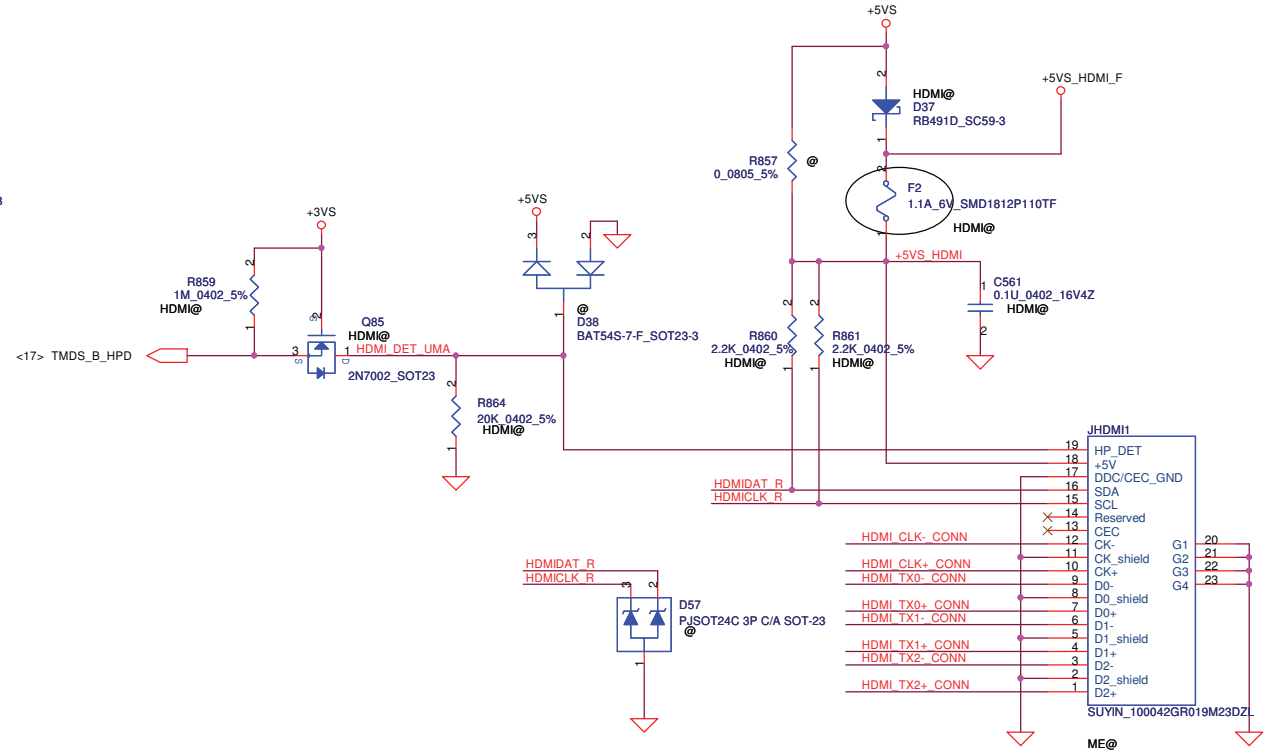
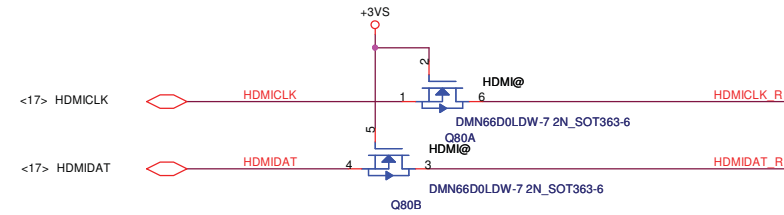




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Size	Custom	Document Number	QIWIY3 LA-8001P	Rev	1.0
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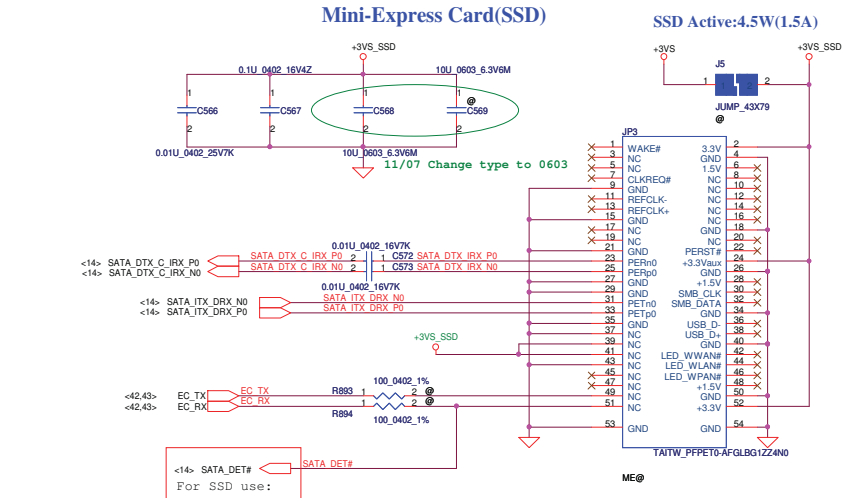
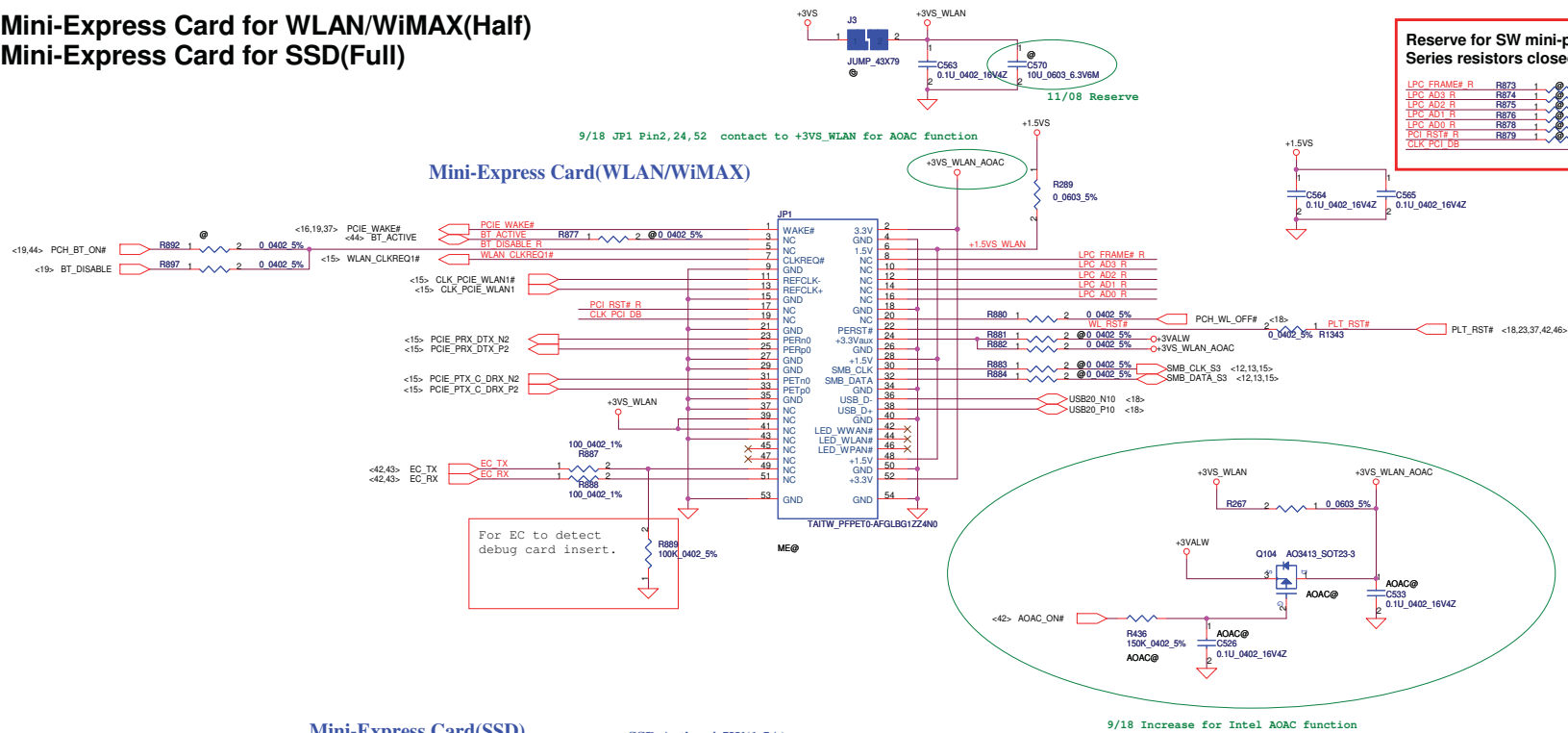


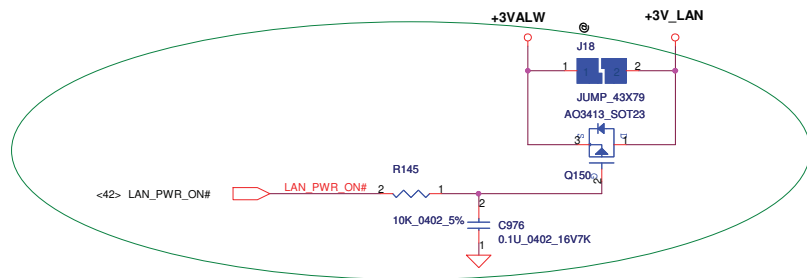
<17>	HDMI_CLK+_CK	R865	1	@	2	0	0402_5%	HDMI_CLK+_CONN
<17>	HDMI_CLK-_CK	R866	1	@	2	0	0402_5%	HDMI_CLK-_CONN
<17>	HDMI_TX0+_CK	R867	1	@	2	0	0402_5%	HDMI_TX0+_CONN
<17>	HDMI_TX0-_CK	R868	1	@	2	0	0402_5%	HDMI_TX0-_CONN
<17>	HDMI_TX1+_CK	R869	1	@	2	0	0402_5%	HDMI_TX1+_CONN
<17>	HDMI_TX1-_CK	R870	1	@	2	0	0402_5%	HDMI_TX1-_CONN
<17>	HDMI_TX2+_CK	R871	1	@	2	0	0402_5%	HDMI_TX2+_CONN
<17>	HDMI_TX2-_CK	R872	1	@	2	0	0402_5%	HDMI_TX2-_CONN



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Size	Custom	Document Number	QIWIY3 LA-8001P	Rev	1.0
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Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

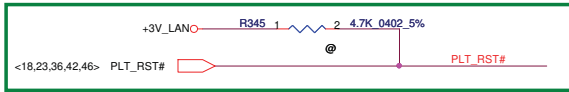




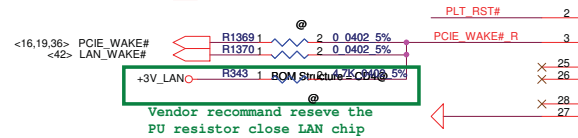
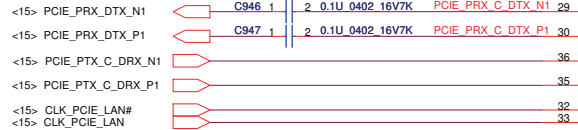
11/08 Increase for LAN S5 power saving

Layout Notice : Place as close chip as possible.

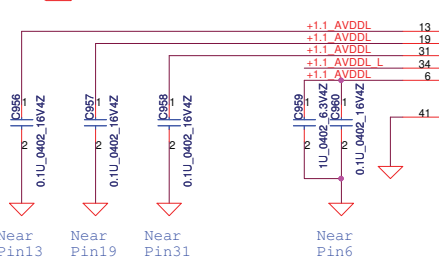
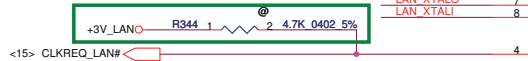
Vendor recommend reseve the PU resistor close LAN chip



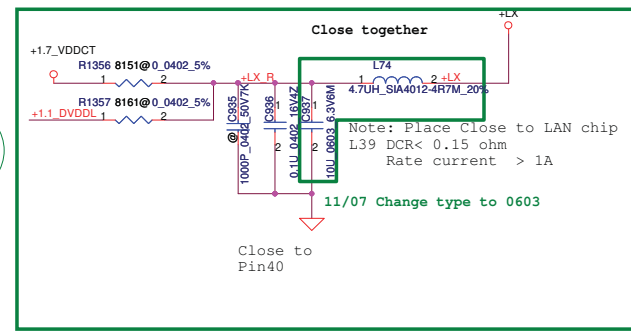
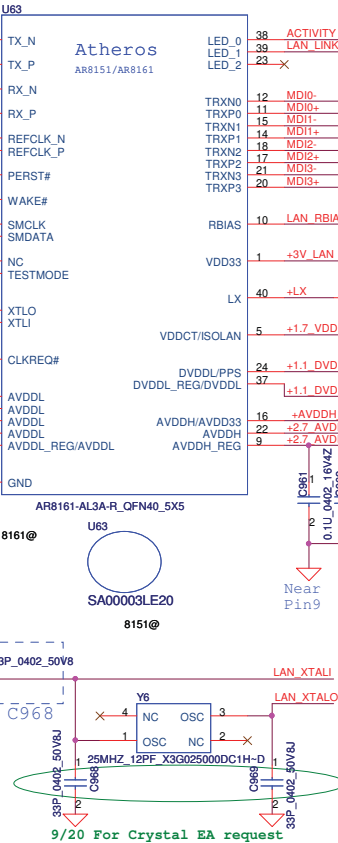
Place Close to Chip



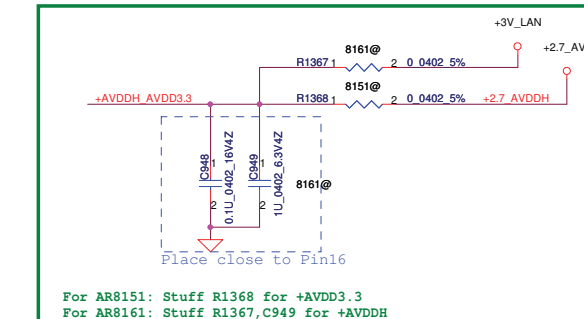
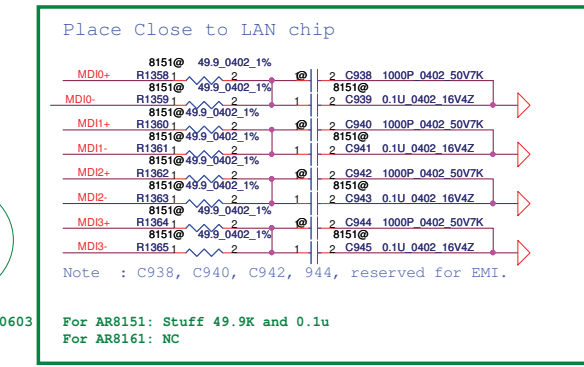
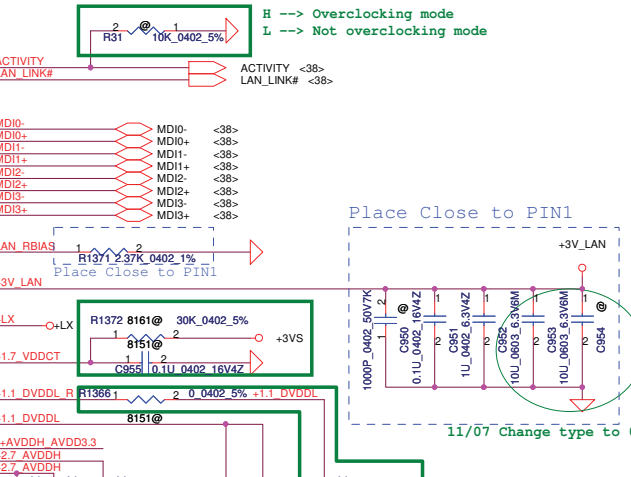
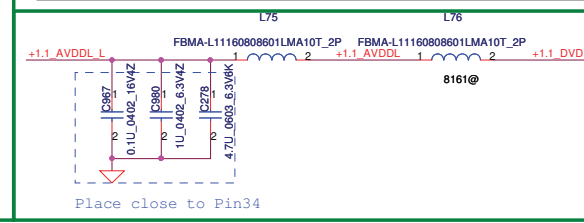
Vendor recommend reseve the PU resistor close LAN chip



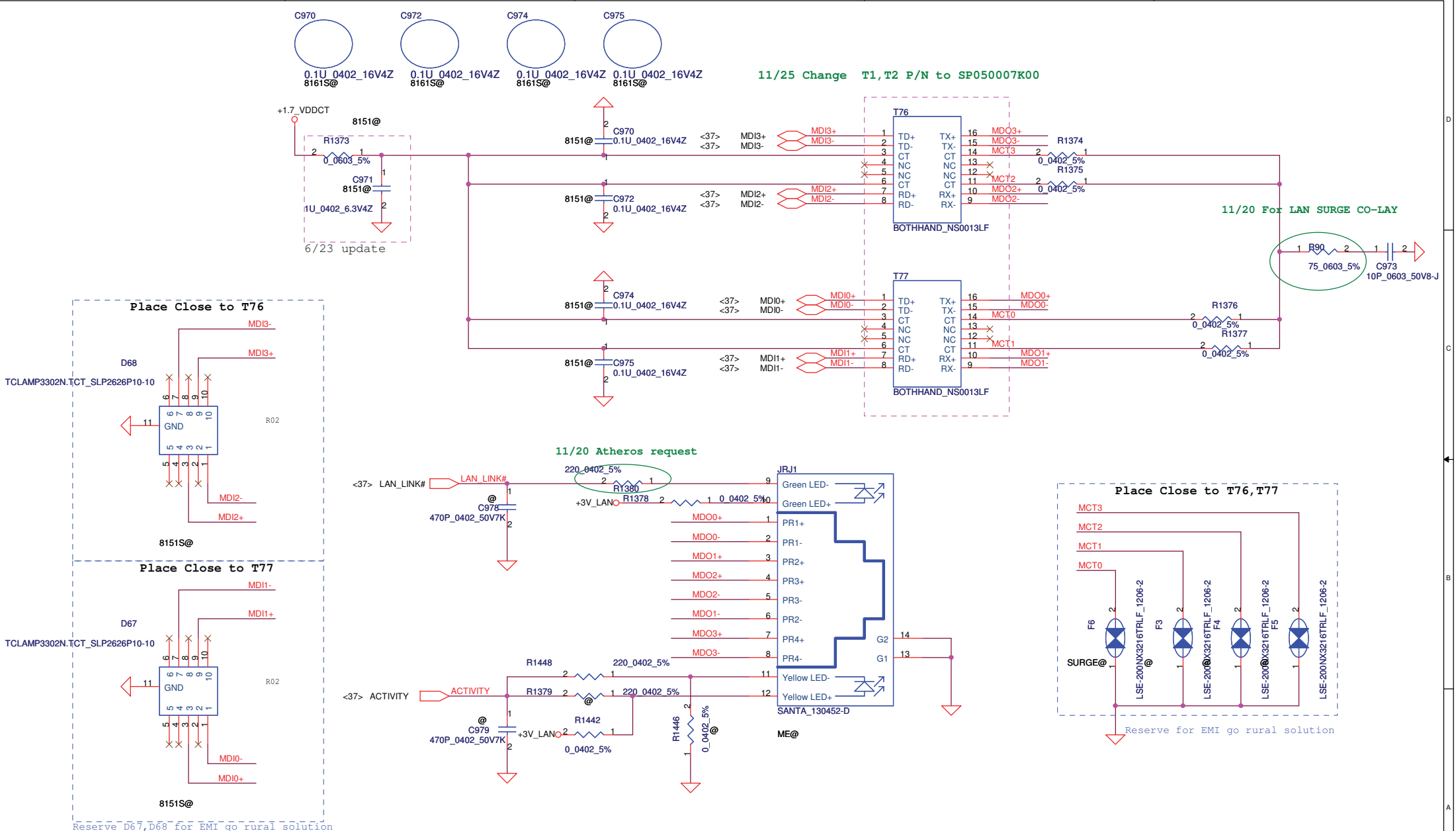
Place Close to C968



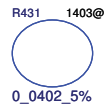
	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76



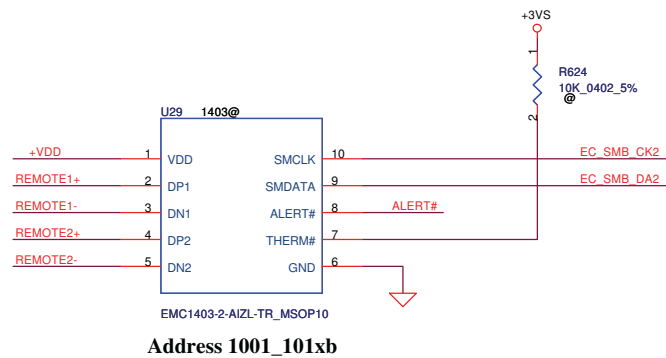
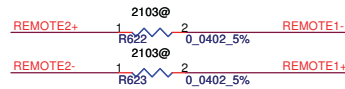
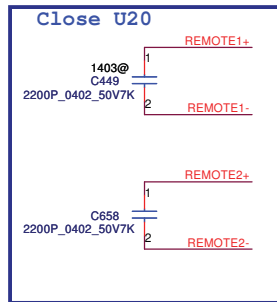
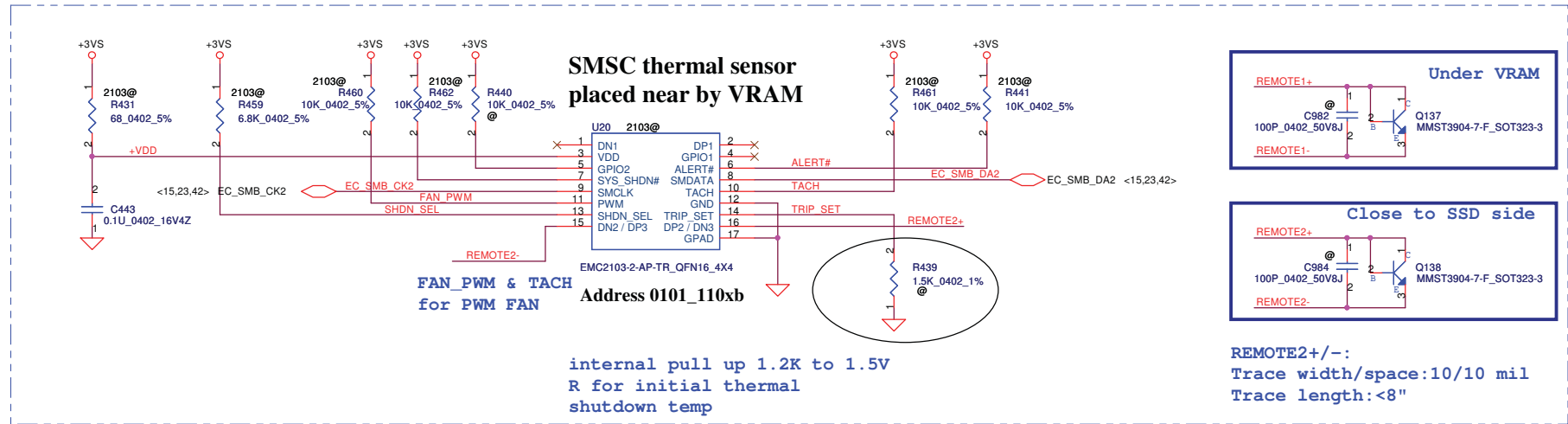
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Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title
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Size	Document Number	QIWI3 LA-8001P	Rev	1.0
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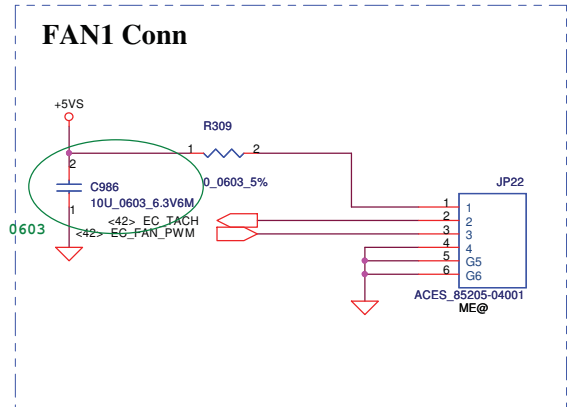
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
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Size	Document Number			Rev	
B	QIWIY3 LA-8001P			1.0	
Date:	Monday, January 16, 2012			Sheet	64
				38	of



1403:
@C982/@C984=100p

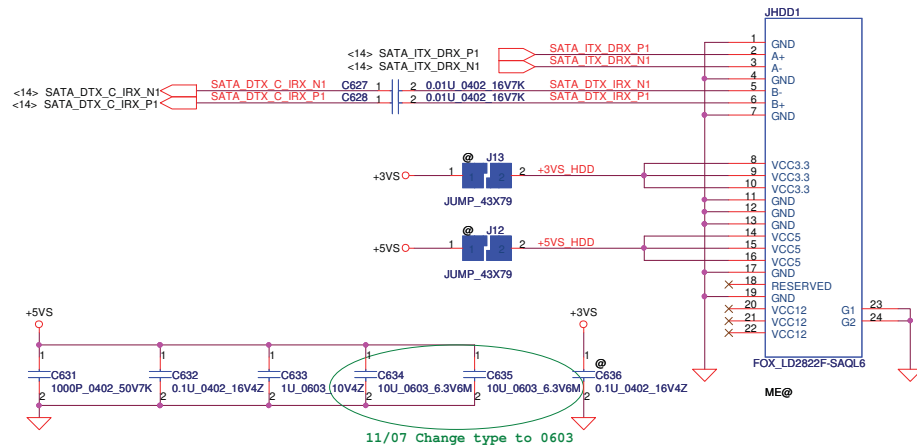


Shutdown Temp	TRIP_SET R1387 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

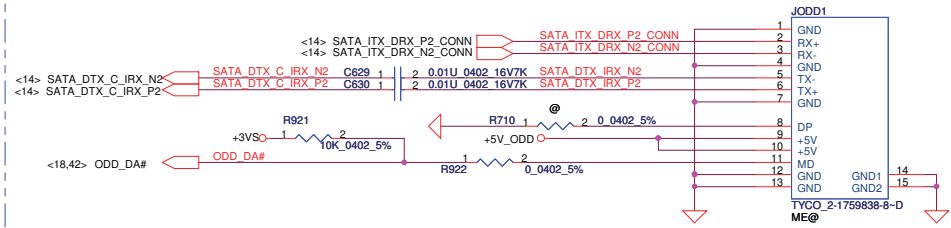


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
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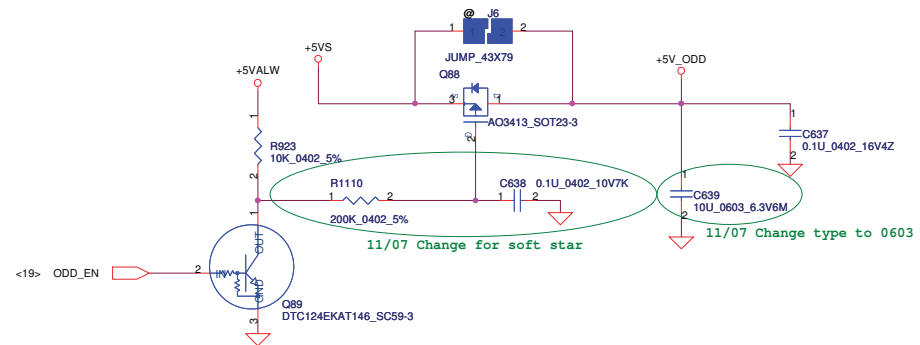
SATA HDD Conn.



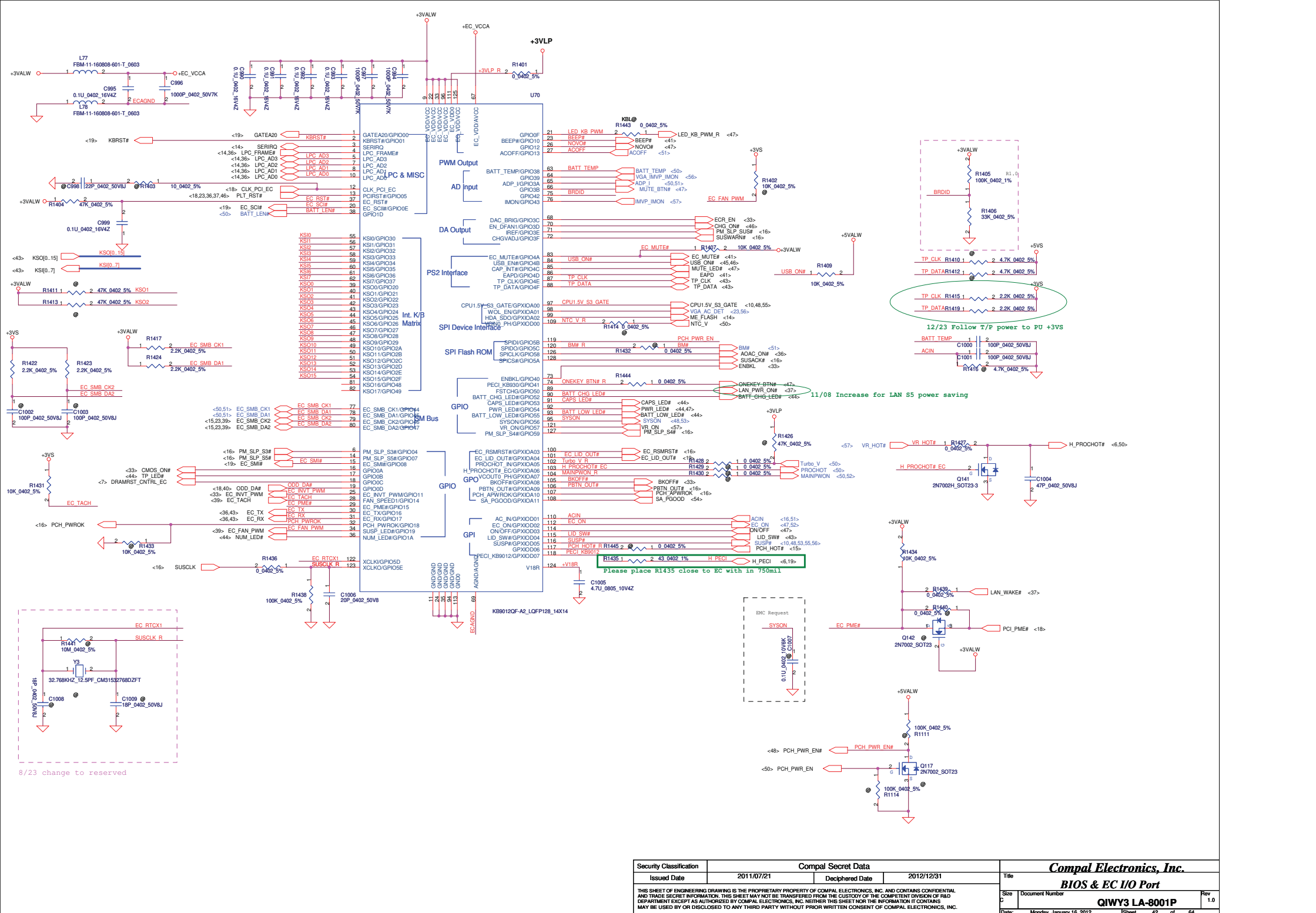
SATA ODD Conn.



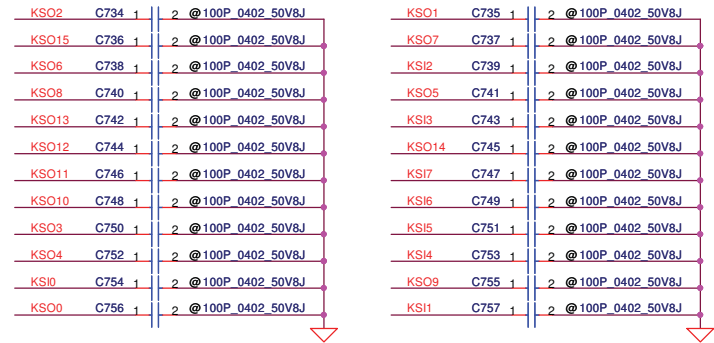
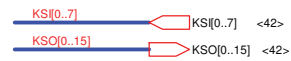
ODD Power Control



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Size B	Document Number	QIY3 LA-8001P		Rev	1.0
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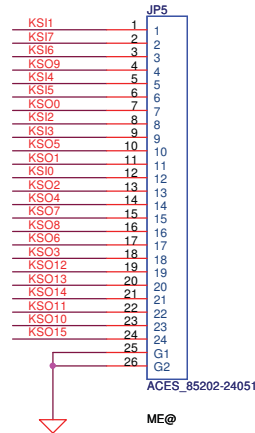
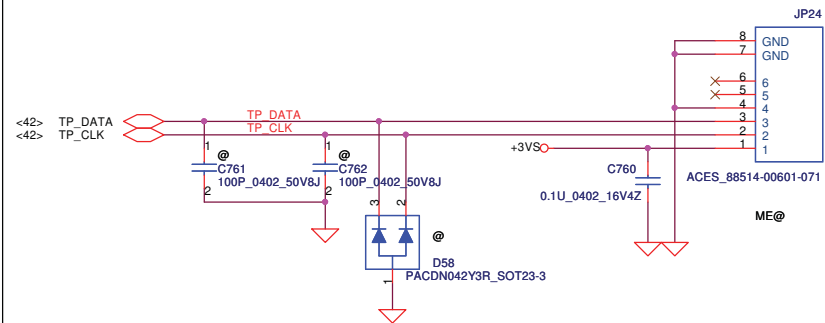


INT_KBD Conn.

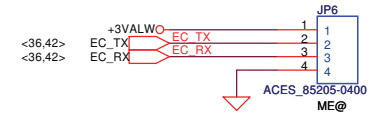


CONN PIN define need double check

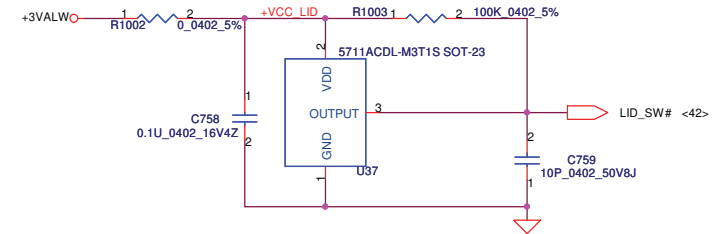
To TP/B Conn.



EC DEBUG PORT

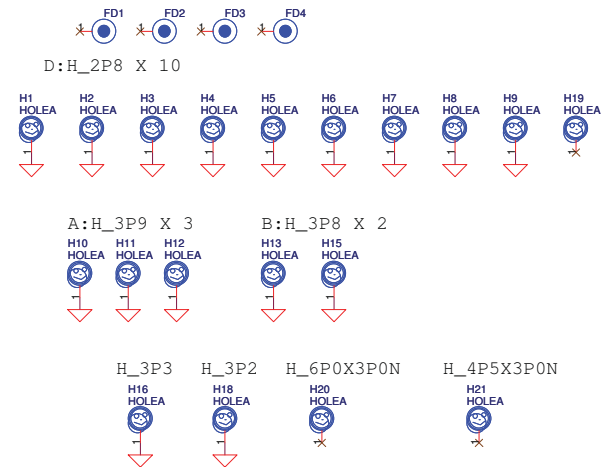
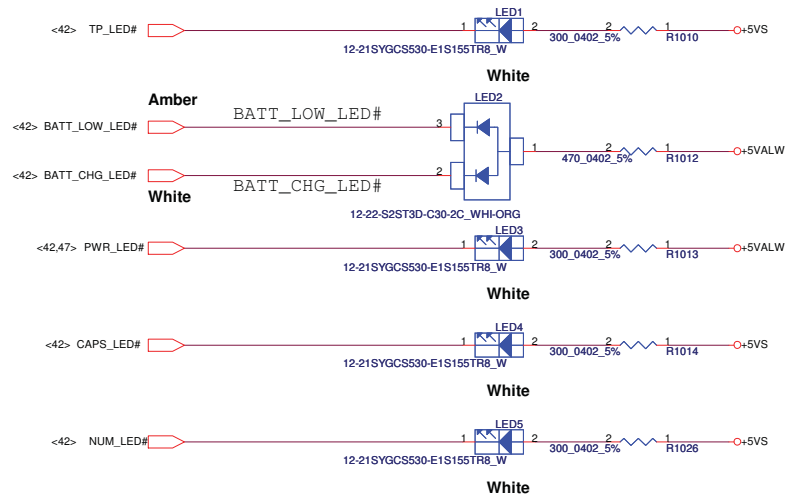


Lid Switch

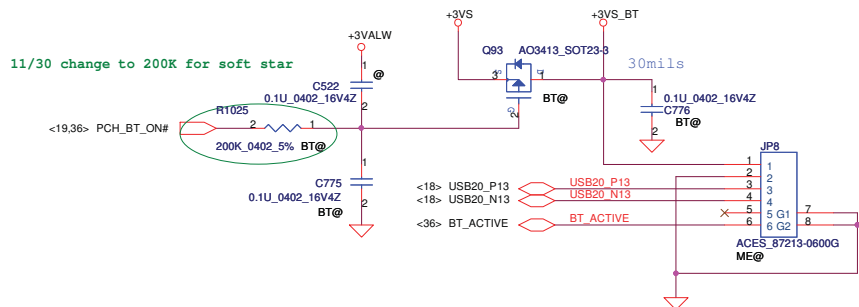


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LED



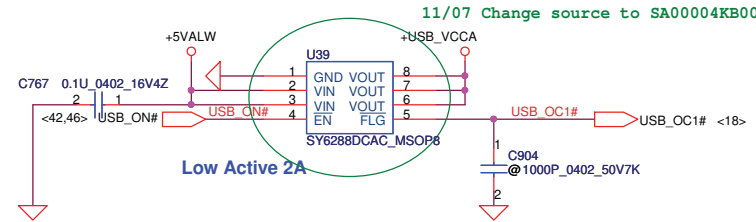
BT MODULE CONN



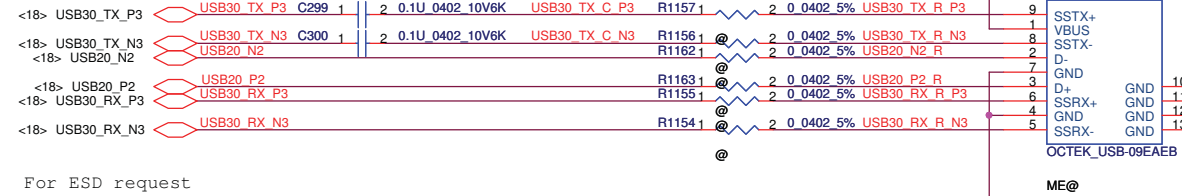
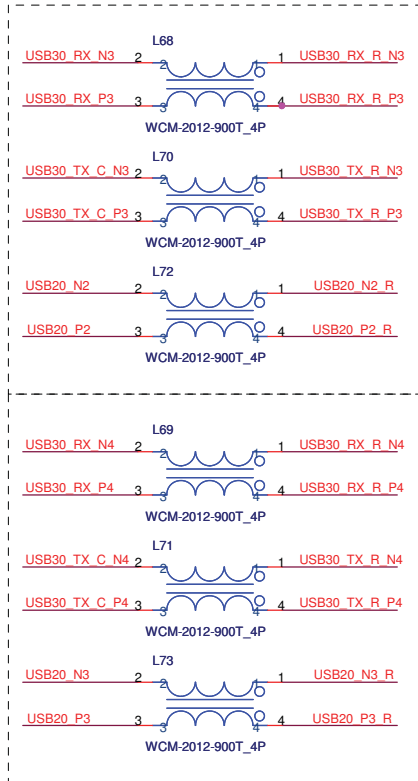
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/07/21		Deciphered Date		2012/12/31		Title	
										LED/EC SPI ROM/BT	
										Size B Document Number	
										QIWIY3 LA-8001P	
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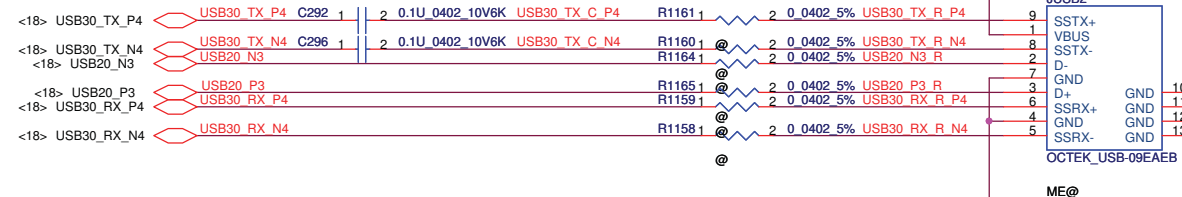
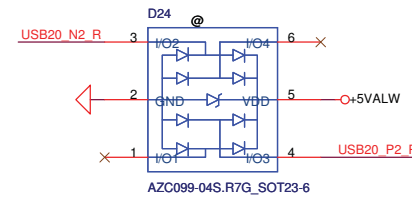
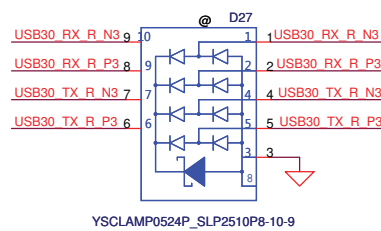
LEFT SIDE USB3.0 PORT X2



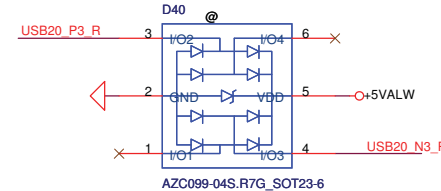
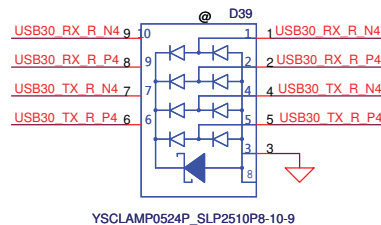
For EMI request
 USB2.0 choke --> SM070000I00
 USB3.0 Choke --> SM070001U00



For ESD request



For ESD request



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11/07 Change source to SA00004KB00

Low Active 2A

CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

USB2.0/3.0 choke and ESD diode at sub-B.

USB2.0/3.0 choke and ESD diode at sub-B.

AC CAP reserve on SUB/B

<18> USB30_TX_P

<18> USB30_TX_N

<18> USB30_RX_P1

<18> USB30_RX_N1

JP23

1

2

3

4

5

6

7

8

9

10

11

12

GND

GND

ACES_50463-0104A-001

ME@

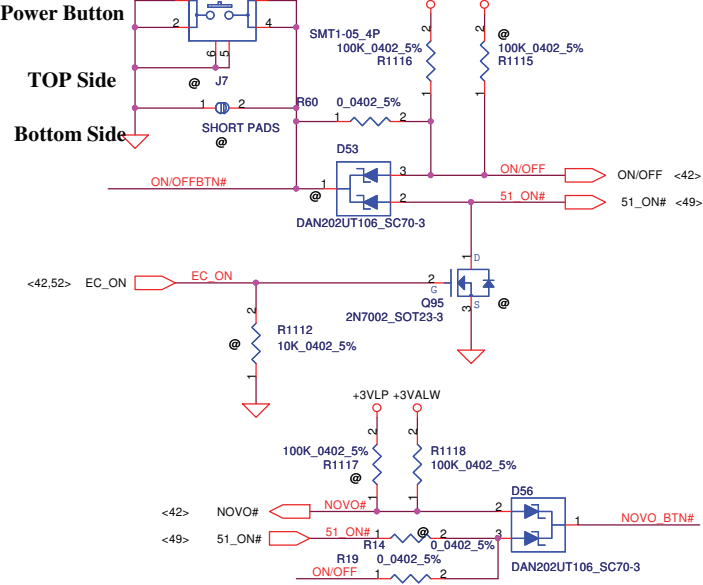
Real USB Conn.(Cable)

The diagram illustrates the internal components and connections of a USB cable. Key components include:

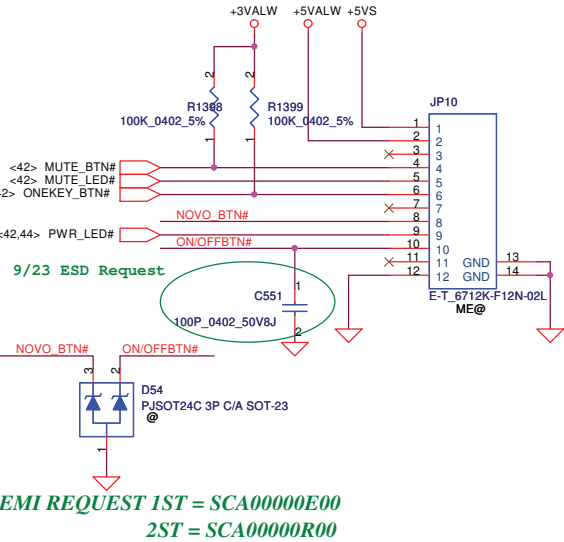
- USB Connector (JUSB3):** A 6-pin connector with pins 1 (D+), 2 (D-), 3 (GND), 4 (GND), 5 (VCC), and 6 (GND).
- USB Cable:** A cable with a length of $W=80\text{mils}$. It contains two twisted pairs: USB20_N9 (D+) and USB20_P9 (D-).
- USB Controller (U40):** A SY6288DCAC_MSOP8 chip. Its pins are connected as follows:
 - Pin 1 (GND) to GND.
 - Pin 2 (VIN) to USB_VCCB.
 - Pin 3 (VIN) to USB_VCCB.
 - Pin 4 (EN) to USB_ON#.
 - Pin 5 (VOUT) to USB_OC4#.
 - Pin 6 (VOUT) to USB_OC4#.
 - Pin 7 (VOUT) to USB_OC4#.
 - Pin 8 (FLG) to USB_OC4#.
- USB Cable Assembly:** A cable with a length of $W=80\text{mils}$. It contains two twisted pairs: USB20_N9 (D+) and USB20_P9 (D-).
- USB Cable Assembly:** A cable with a length of $W=80\text{mils}$. It contains two twisted pairs: USB20_N9 (D+) and USB20_P9 (D-).
- USB Cable Assembly:** A cable with a length of $W=80\text{mils}$. It contains two twisted pairs: USB20_N9 (D+) and USB20_P9 (D-).

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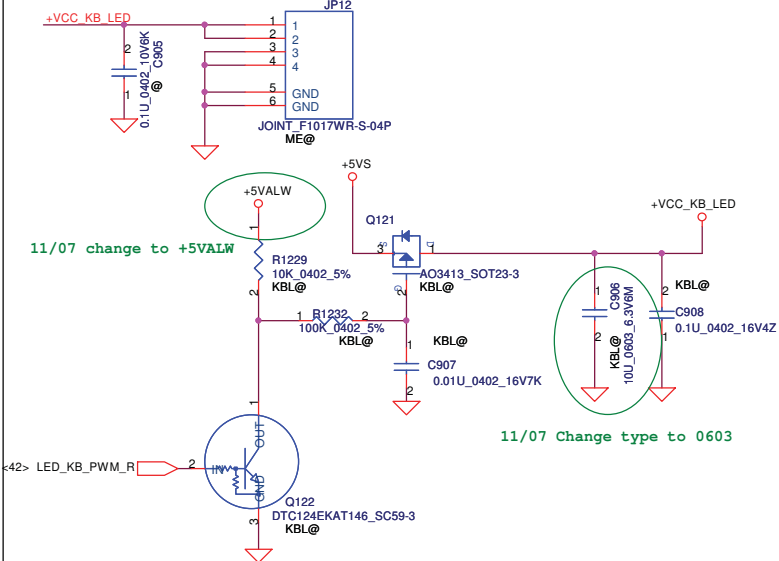
ON/OFF switch



Power Button/B link to Function/B Conn. 10pin



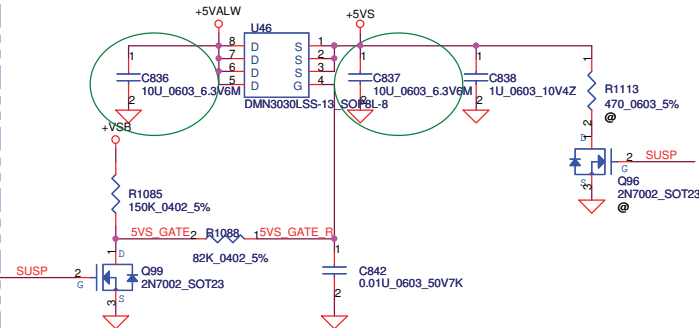
KB Lighting CONN.4pin



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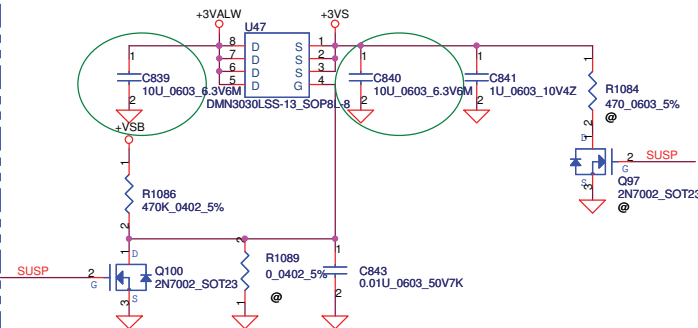
+5VALW TO +5VS

11/07 Change type to 0603



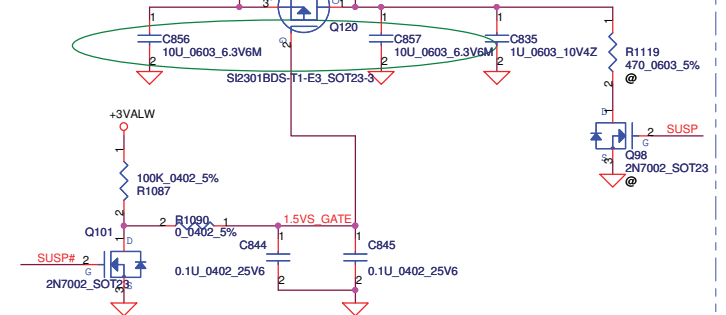
+3VALW TO +3VS

11/07 Change type to 0603



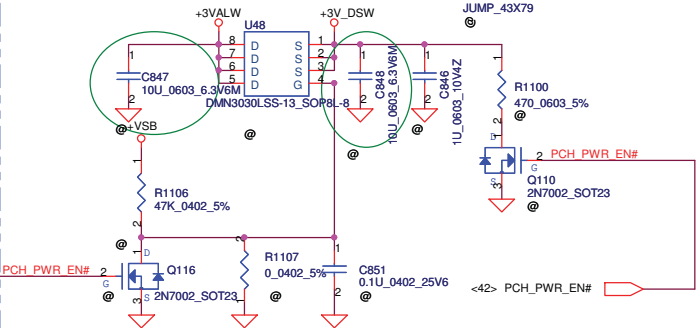
+1.5V to +1.5VS

11/07 Change type to 0603



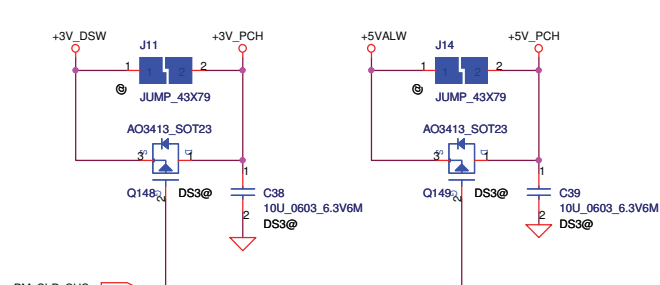
+3VALW TO +3V_DSW

11/07 Change type to 0603

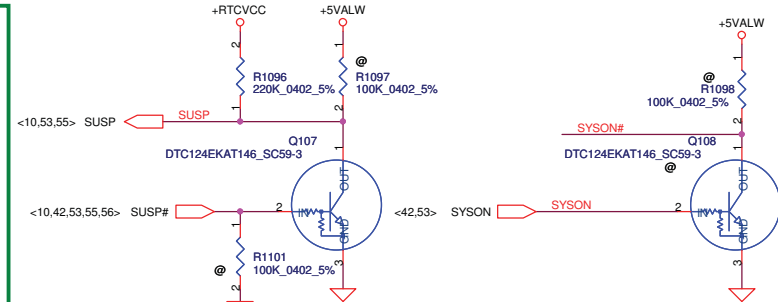


+3V_DSW to +3V_PCH

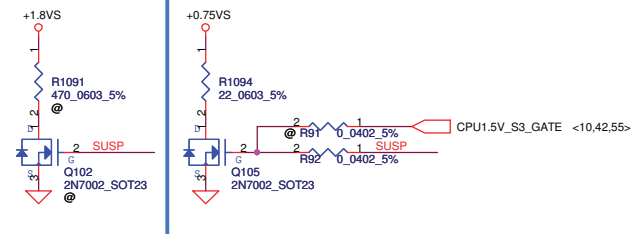
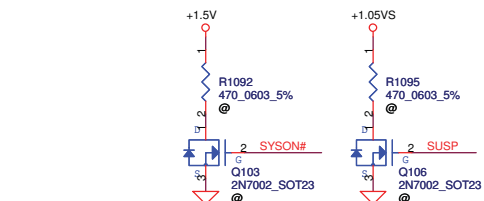
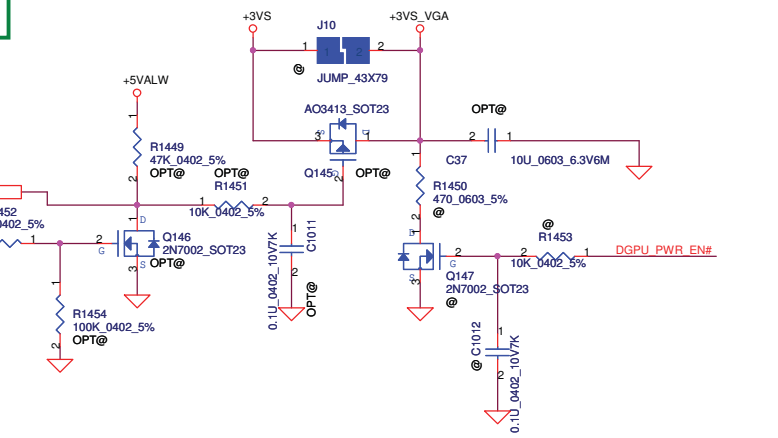
+5VALW to +5V_PCH



09/05 add for Deep S3



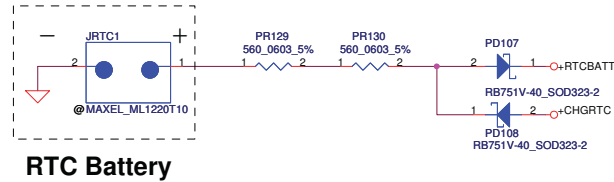
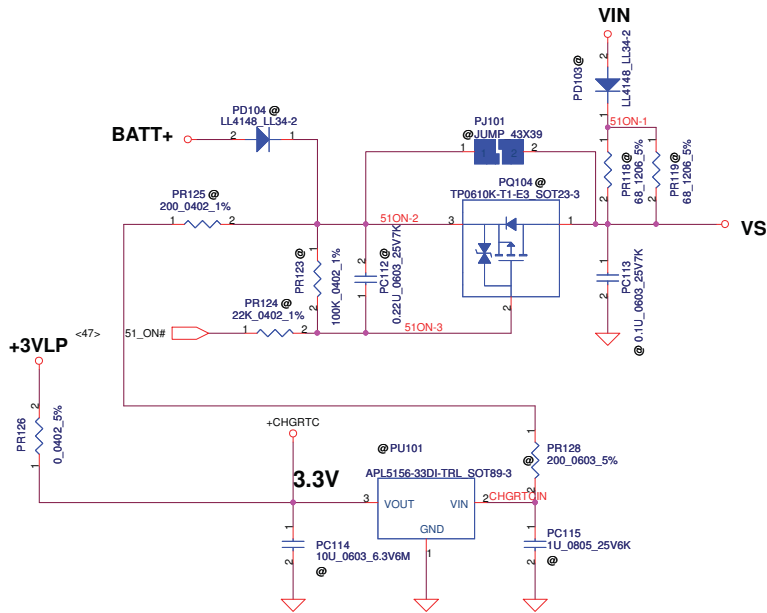
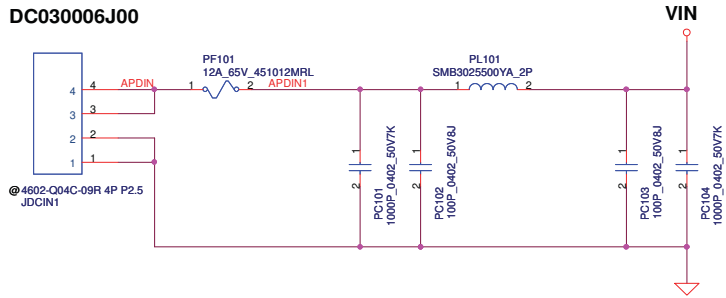
+3VS to +3VS_VGA



For Intel S3 Power Reduction.

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						Size		Document Number		Rev	
						Custom		QIWIY3 LA-8001P		1.0	
						Date:		Monday, January 16, 2012		Sheet 48 of 64	

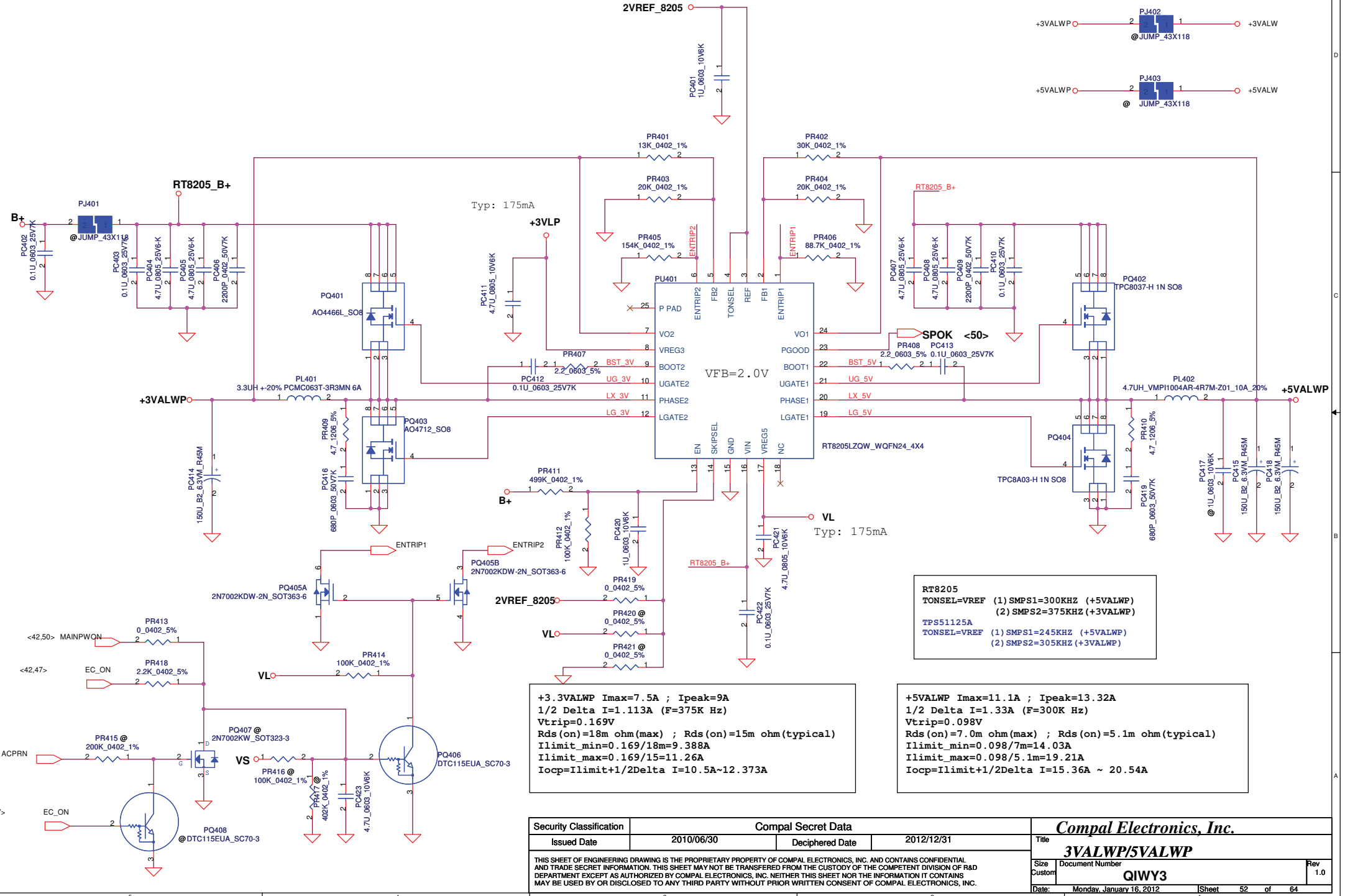
DC030006J00



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				Custom	1.0
				Date:	Monday, January 16, 2012
				Sheet	49 of 64

[illegible]

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



+3.3VALWP I_{max}=7.5A ; I_{peak}=9A
1/2 Delta I=1.113A (F=375K Hz)
V_{trip}=0.169V
R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
I_{limit_min}=0.169/18m=9.388A
I_{limit_max}=0.169/15=11.26A
I_{ocp}=I_{limit}+1/2Delta I=10.5A~12.373A

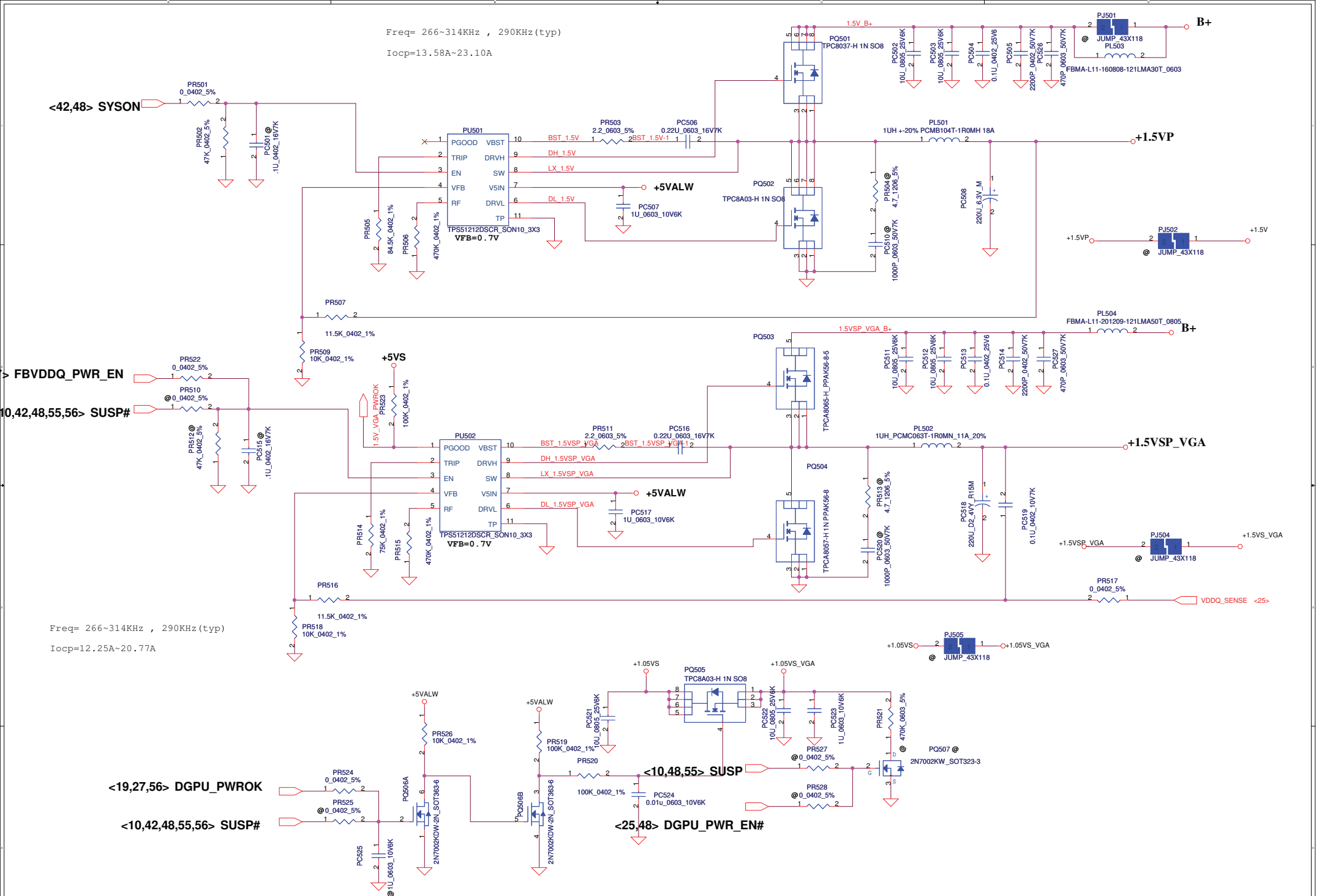
RT8205
T_{ONSEL}=V_{REF} (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)
TPS51125A
T_{ONSEL}=V_{REF} (1) SMPS1=245KHZ (+5VALWP)
(2) SMPS2=305KHZ (+3VALWP)

+5VALWP I_{max}=11.1A ; I_{peak}=13.32A
1/2 Delta I=1.33A (F=300K Hz)
V_{trip}=0.098V
R_{ds(on)}=7.0m ohm(max) ; R_{ds(on)}=5.1m ohm(typical)
I_{limit_min}=0.098/7m=14.03A
I_{limit_max}=0.098/5.1m=19.21A
I_{ocp}=I_{limit}+1/2Delta I=15.36A ~ 20.54A

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				Date	Monday, January 16, 2012
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Freq= 266~314KHz , 290KHz(typ)

Iocp=13.58A~23.10A



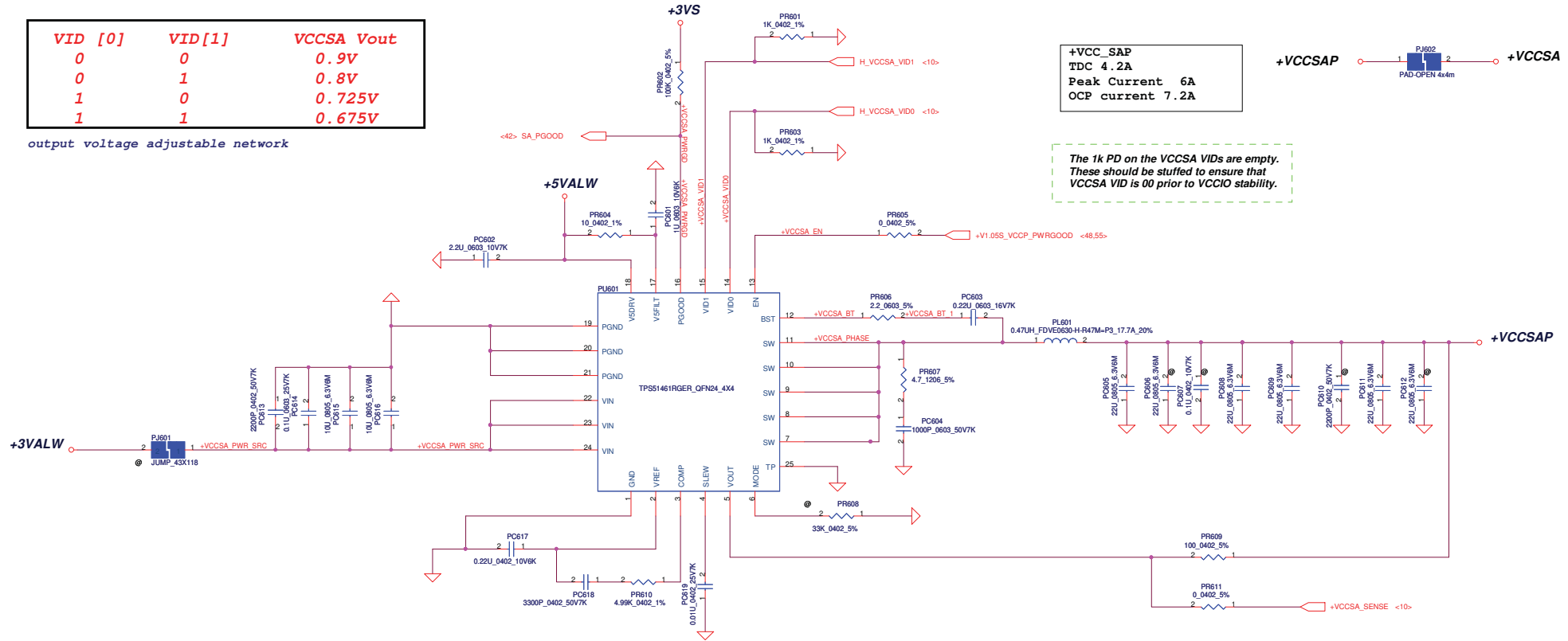
Freq= 266~314KHz , 290KHz(typ)

Iocp=12.25A~20.77A

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								1.5VP/1.5VSP_VGA/1.05VSP_VGA	
								Size Document Number	
								QIWIY3	
								Rev 1.0	
								Date: Monday, January 16, 2012	
								Sheet 53 of 64	

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

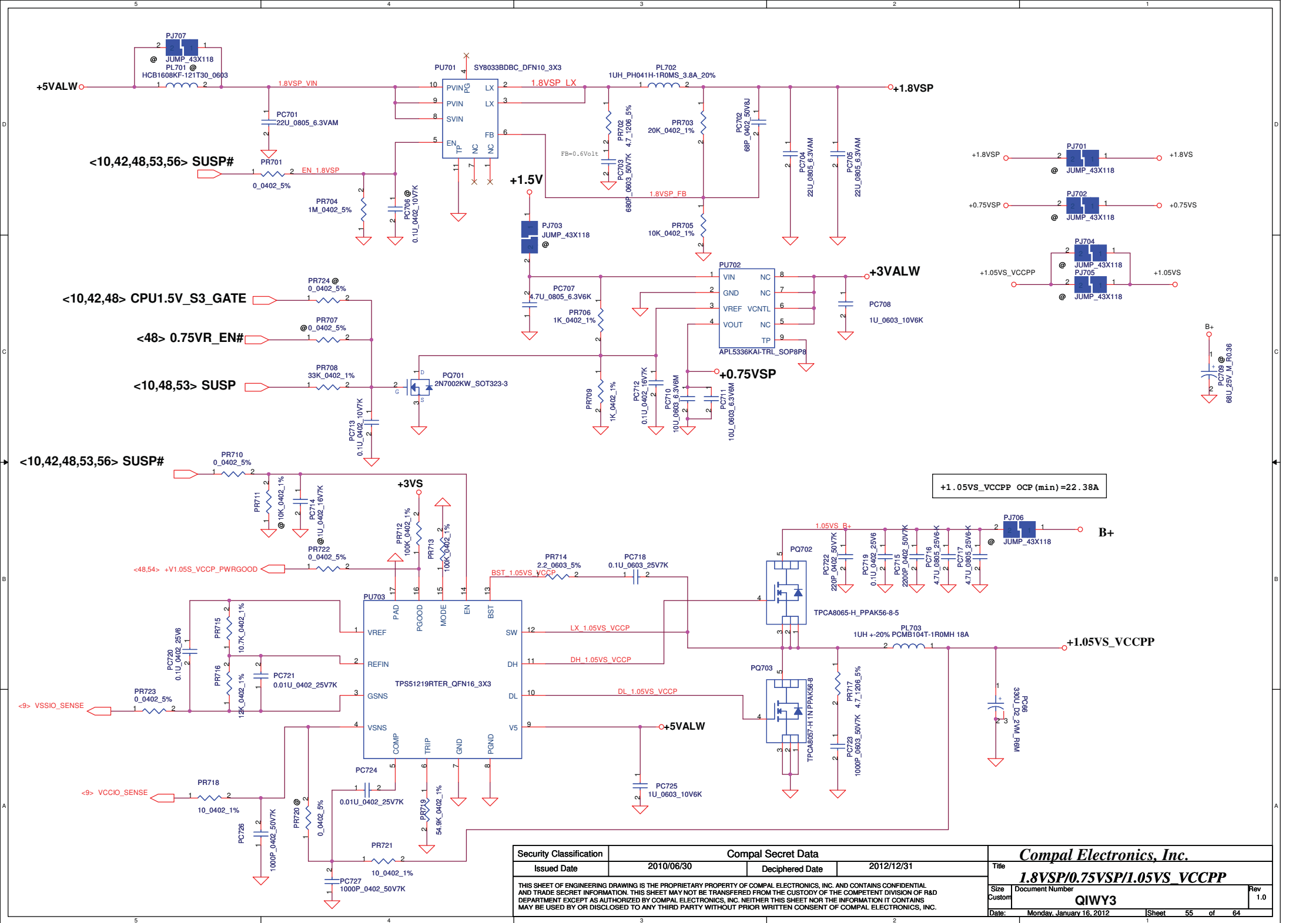
output voltage adjustable network



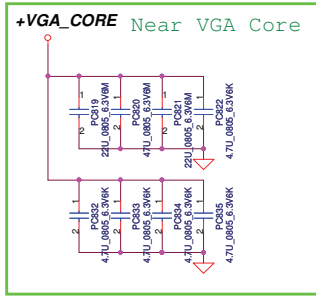
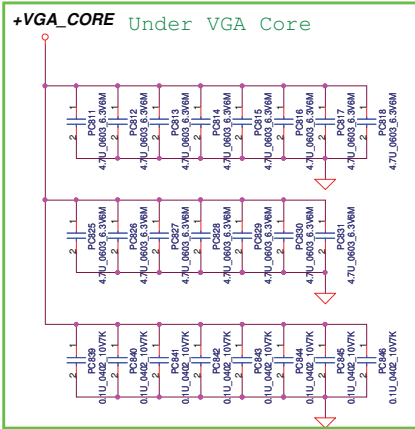
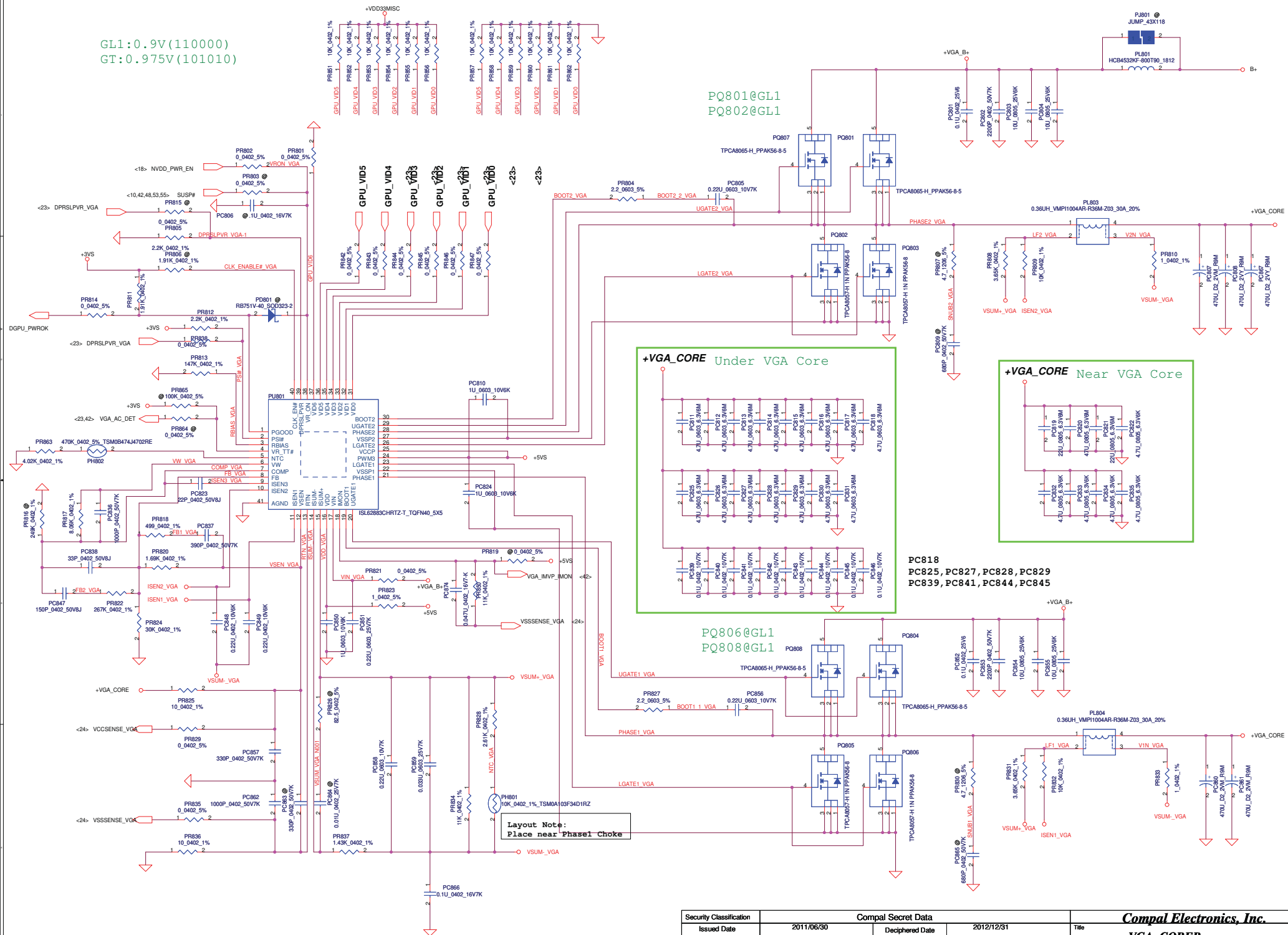
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

+VCCSAP P1602 PAD OPEN 4x4m +VCCSA

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

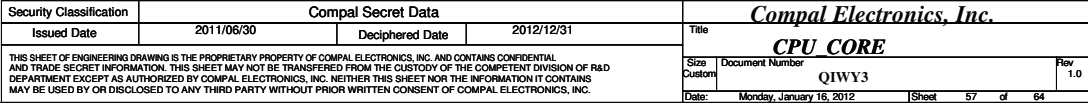


GL1:0.9V(110000)
GT:0.975V(101010)



Layout Note:
Place near Phase1 Choke

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2011/06/30		2012/12/31		Rev 1.0	
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Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	2011/09/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470pF)	2011/09/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	2011/09/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	2011/09/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	2011/09/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	2011/09/27	B test
7	for CPU_CORE load line adjust	57	add PC969	2011/09/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	2011/09/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	2011/09/27	B test
10	for debug	51	add PR329,PR330	2011/11/30	C test
11	for VCCIO remote sense	55	add PR723	2011/11/30	C test
12	RC filter to reduce noise	55	add PR721,PC727	2011/11/30	C test
13	G718 for adapter and OTP	50	pop PC203,PQ201,PR209,PU201,PR213 unpop PR206	2011/11/30	C test
14	for CPU transient	58	change PR911,PR912 to 91K	2011/11/30	C test
15	for EMI Request		add PL301,PC503,PL504,PL801 add PC302,PC323,PC424,PC526,PC722,PC970,PC974	2011/11/30	C test
16	HW request	50 55	reserve connect PCH_PWR_EN for power sequence reserve connect CPU1.5V_S3_GATE for power sequence	2011/11/30	C test
17	for thermal request to reduce temperature	53	change PQ503,PQ504	2011/11/30	C test
18	adjust 1.5VSP_VGA OCP	53	change PR514 to 49.9K	2011/11/30	C test
19	For HW power sequence adjustment	50	change PR222,PR228 to NA change PR229 to 0 ohm	2011/12/02	C test
20	To adjust +5VALW by HW request	52	change PR404 to 19.6K	2011/12/16	C test
21	Using G718 to replace KB9012 function need to add or reserve resistor	50	Add PR232 and reserve PR233 pull high to +3VALW Add PR234 pull down	2011/12/28	Pre MP

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2011/06/30		2012/12/31		PIR (PWR)	
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	S		4		3		2		1
QIWY3 HW PIR List									
No	Date	Page	Modification List		Purpose				
						----- EVT TO DVT			
1		P7	Reserve R64		Reserve EC DRAMRST control pin for Deep S3				
2		P16	Reserve R1457,R1455,R1447		Reserve SUSACK#,SUSWARN#,SLP_SUS# control signal for Deep S3				
3		P16	Reserve Q118,R1120,R1121		Reverse SLP_SUS# to control +3V_PCH&+5V_PCH				
4		P16	Change AC_PRESENT Pull high source to +3V_DSW		For Deep S3 function				
5		P21	Remove R289		+5V_PCH control circuit change for Deep S3				
6		P36	Reserve J8,Q104,C533,C526,R436		Reserve for AOAC function				
7		P36	Change JP1 pin2,24,52 power source to +3VS_WLAN_AOAC		Reserve for AOAC function				
8		P42	Change EC GPIO pin setting (Impact pin 18,71,72,126,128)		For DeepS3/AOAC function				
9		P48	Reserve J11,J14,Q148,Q149,C38,C39		+3V_PCH&+5V_PCH control circuit for Deep S3				
10		P45	change U49 symbol (without GND pad)		For DFx issue				
11		P46	change U40,U69 symbol (without GND pad)		For DFx issue				
12		P47	change JP10 type to SP01001B800		For DFx issue				
13		P19	Reserve R207,R224 to contact WLAN wake even		Reserve for AOAC function				
14		P41	Change JSPK1 type to SP02000H700		For DFx issue				
14		P19	Reserve R704 and R706 for GPIO69 PU&PD		For SKU ID				
15		P23	Change CV37,CV38 to 22P		For Crystal EA request				
16		P37	Change C968,C969 to 33P		For Crystal EA request				
						----- DVT TO PVT			
1		P14	Change power source to +5VS (Q10 pin 2)		Follow intel Design Guide				
2		P16	Reserve R257 PU 10K to +3V_DSW		For Deep S3 function				
3		P40	Change R1110 to 200K,C638 to 0.1u		For ODD soft star				
4		P10	Change C124,C125,C126,C127,C130 to 0603 type		For common design				
5		P20	Change C215,C221,C395 to 0603 type		For common design				
6		P21	Change C231 to 0603 type		For common design				
7		P33	Change C519 to 0603 type		For common design				
8		P36	Change C568,C569 to 0603 type		For common design				
9		P37	Change C937,C954,C953 to 0603 type		For common design				
10		P39	Change C986 to 0603 type		For common design				
11		P40	Change C634,C635,C639 to 0603 type		For common design				
12		P41	Change C655 to 0603 type		For common design				
13		P48	Change C836,C837,C839,C840,C847 C848,C856,C857 to 0603 type		For common design				
14		P47	Change C906 to 0603 type		For common design				
15		P47	Modify gate powr rail of MOS to +5VALW		Avoid leakage issue.				
16		P45	Change U39 source to SA00004KB00		For main source issue				
17		P46	Change U40,U69 source to SA00004KB00		For main source issue				
18		P37	Add Q150,R145,C976		For LAN power control				
19		P42	Reserve LAN_PWR_ON# net on EC pin 89		For LAN power control				
20		P41	Stuff R945,R481 for EAPD contact U8 pin29		For MUTE_LED issue				
21		P38	Add R90		For LAN SUR				

QIWIY3 HW PIR List					
NO DATE	PAGE	MODIFICATION LIST		PURPOSE	
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3	P16	Reserve Q118,R1120,R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH		
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5	P21	Remove R289	+5V_PCH control circuit change for Deep S3		
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8	P42	Change EC GPIO pin setting (Impact pin 18,71,72,126,128)	For DeepS3/AOAC function		
9	P48	Reserve J11,J14,Q148,Q149,C38,C39	+3V_PCH&+5V_PCH control circuit for Deep S3		
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14	P41	Change JSPK1 type to SP02000H700	For DFx issue		
14	P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID		
15	P23	Change CV37,CV38 to 22P	For Crystal EA request		
16	P37	Change C968,C969 to 33P	For Crystal EA request		
----- DVT TO PVT					
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2	P16	Reserve R257 PU 10K to +3V_DSW	For Deep S3 function		
3	P40	Change R1110 to 200K,C638 to 0.1u	For ODD soft star		
4	P10	Change C124,C125,C126,C127,C130 to 0603 type	For command design		
5	P20	Change C215,C221,C395 to 0603 type	For command design		
6	P21	Change C231 to 0603 type	For command design		
7	P33	Change C519 to 0603 type	For command design		
8	P36	Change C568,C569 to 0603 type	For command design		
9	P37	Change C937,C954,C953 to 0603 type	For command design		
10	P39	Change C986 to 0603 type	For command design		
11	P40	Change C634,C635,C639 to 0603 type	For command design		
12	P41	Change C655 to 0603 type	For command design		
13	P48	Change C836,C837,C839,C840,C847 C848,C856,C857 to 0603 type	For command design		
14	P47	Change C906 to 0603 type	For command design		
15	P47	Modify gate powr rail of MOS to +5VALW	Avoid leakage issue.		
16	P45	Change U39 source to SA00004KB00	For main source issue		
17	P46	Change U40,U69 source to SA00004KB00	For main source issue		
18	P37	Add Q150,R145,C976	For LAN power control		
19	P42	Reserve LAN_PWR_ON# net on EC pin 89	For LAN power control		
20	P41	Stuff R945,R481 for EAPD contact U8 pin29	For MUTE_LED issue		
21	P38	Add R90	For LAN SURGE CO-LAY		
22	P38	Add R1380	Atheros request		
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QIWEY3 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1		P46	change JP21 type (SP010011A00)	For ASSY issue
2		P23	RV208 change to contact +VDD33MISC	For N13P-GT/N13E-GE shutdown issue
3		P23	Reserve RV14	For N13P-GT/N13E-GE +VDD33MISC leakage issue
4		P41	Swap HP R/L	For HP R/L reverse issue
5		P42	Add R1415, R1419	T/P SM BUS pull high voltage change

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